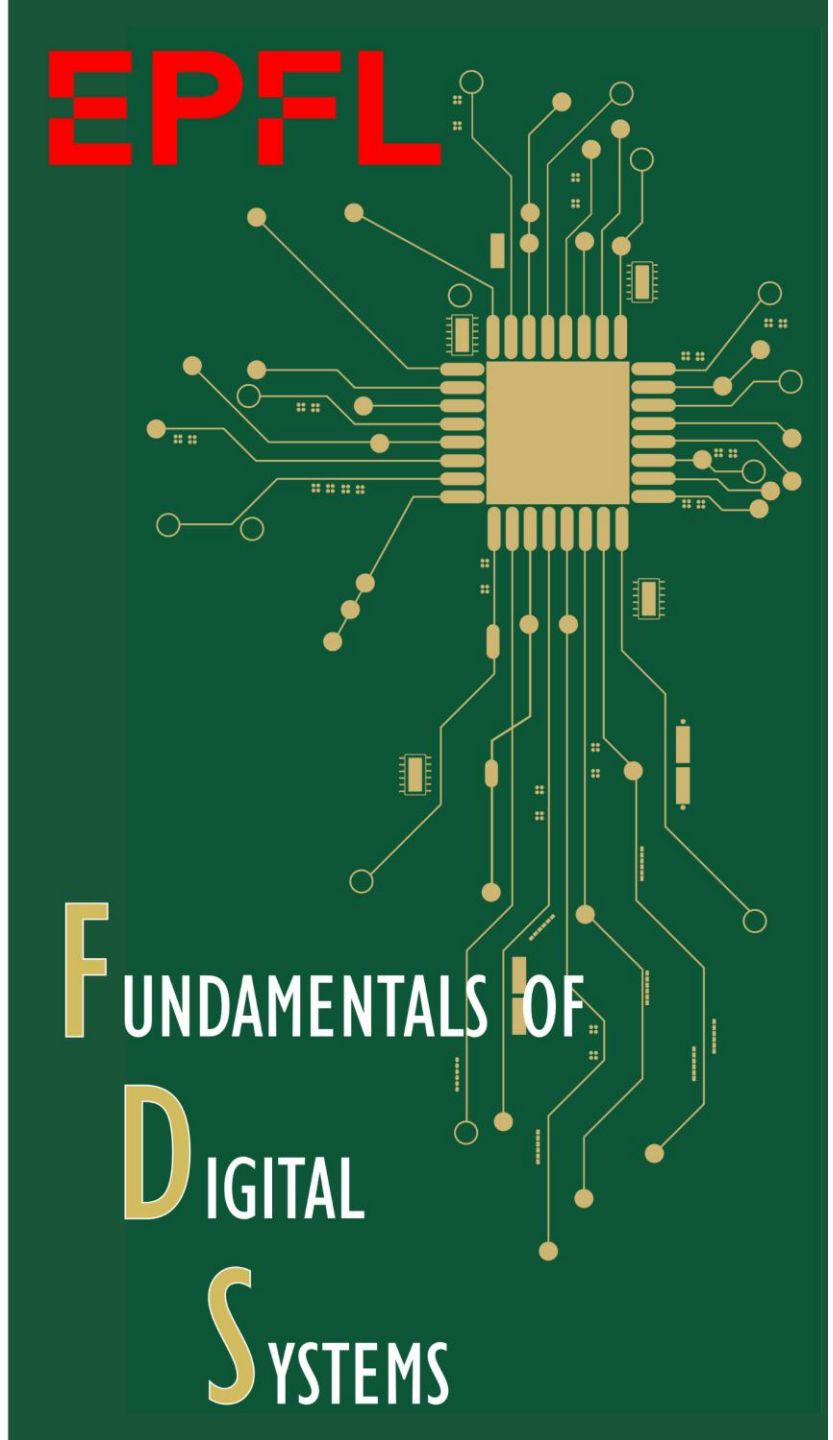


Digital Logic Circuits

Implementation Technology

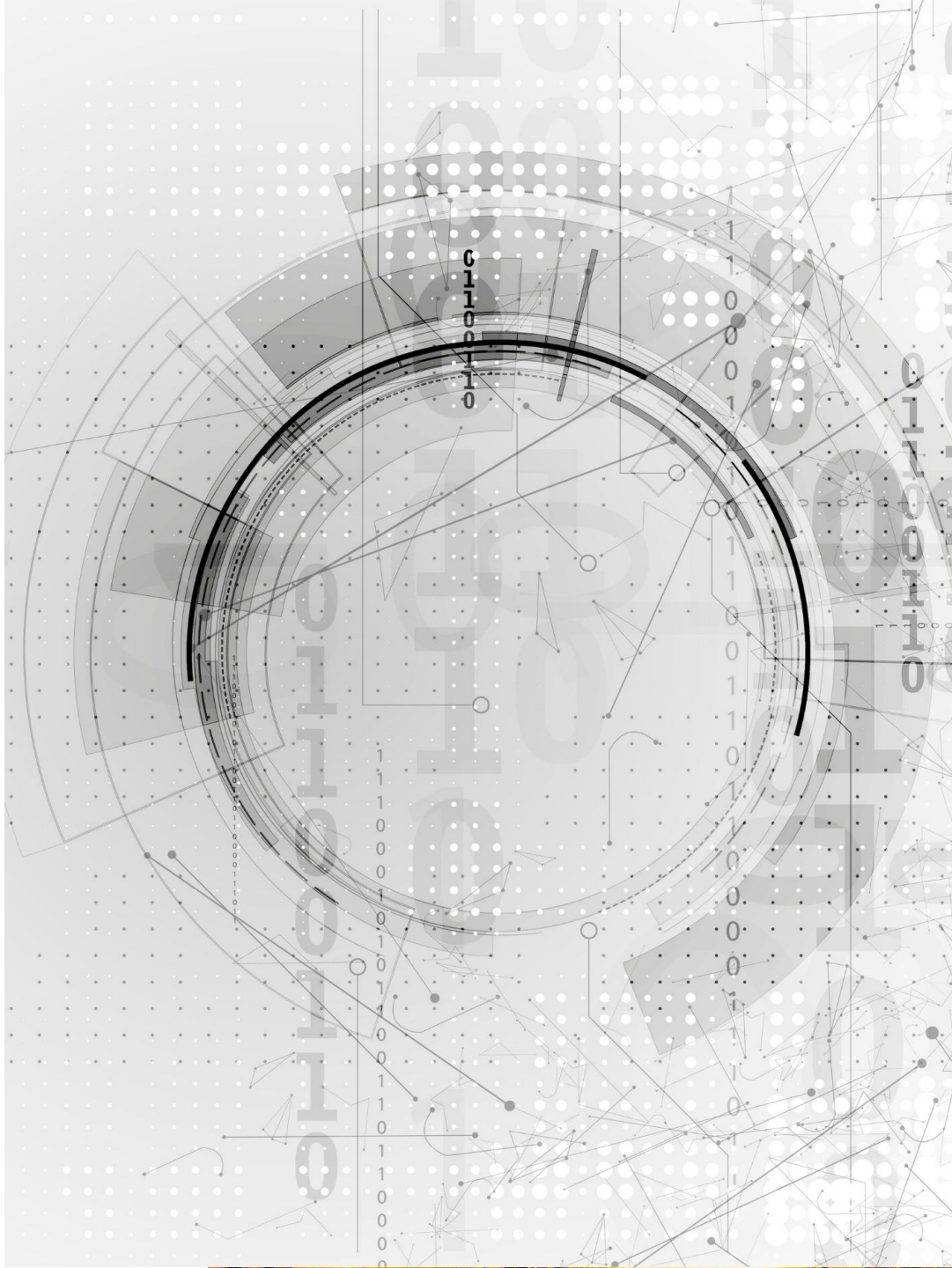
CS-173 Fundamentals of Digital Systems

Mirjana Stojilović

Spring 2025

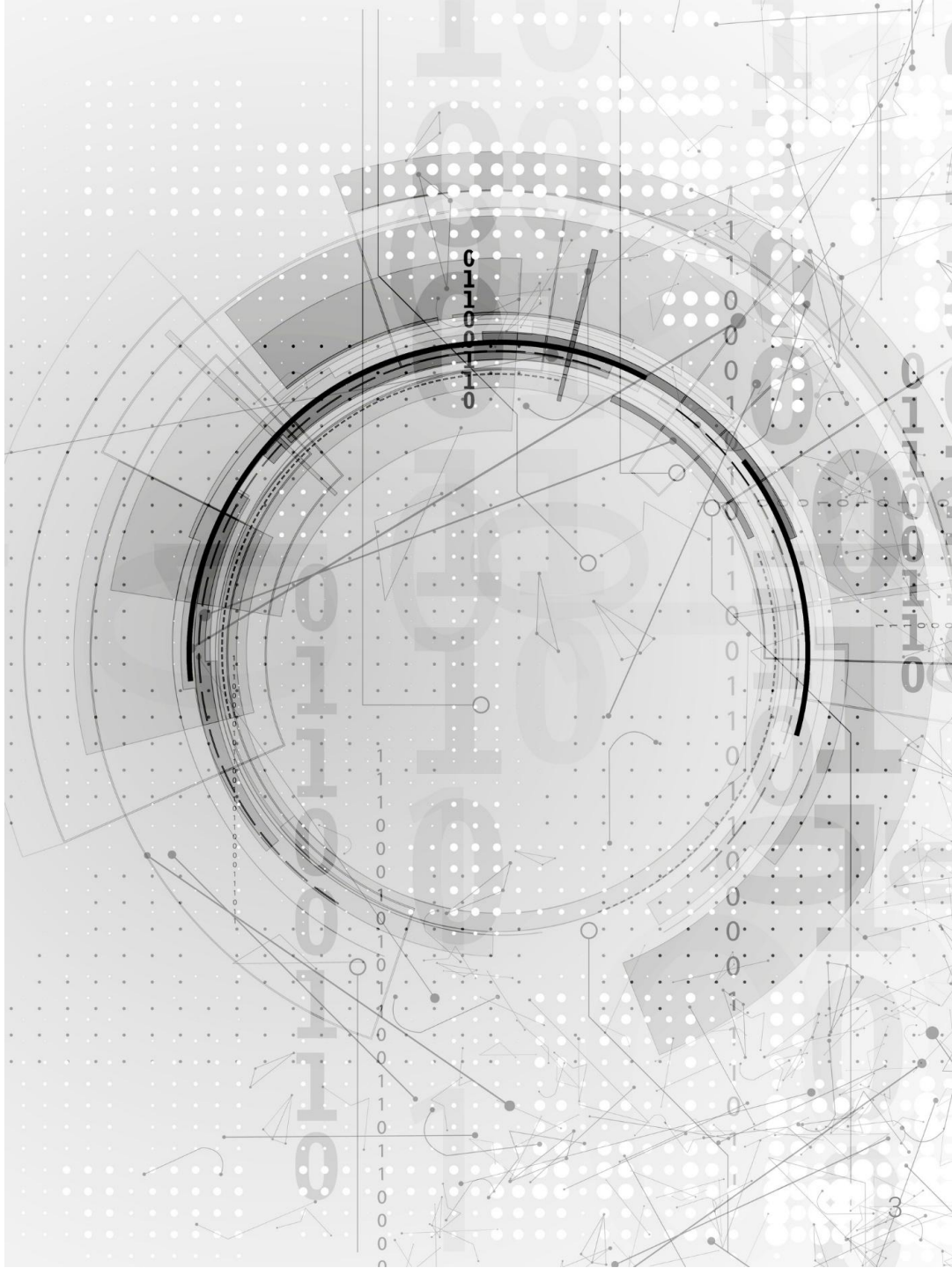
Previously on FDS

Verilog for Combinational Circuits



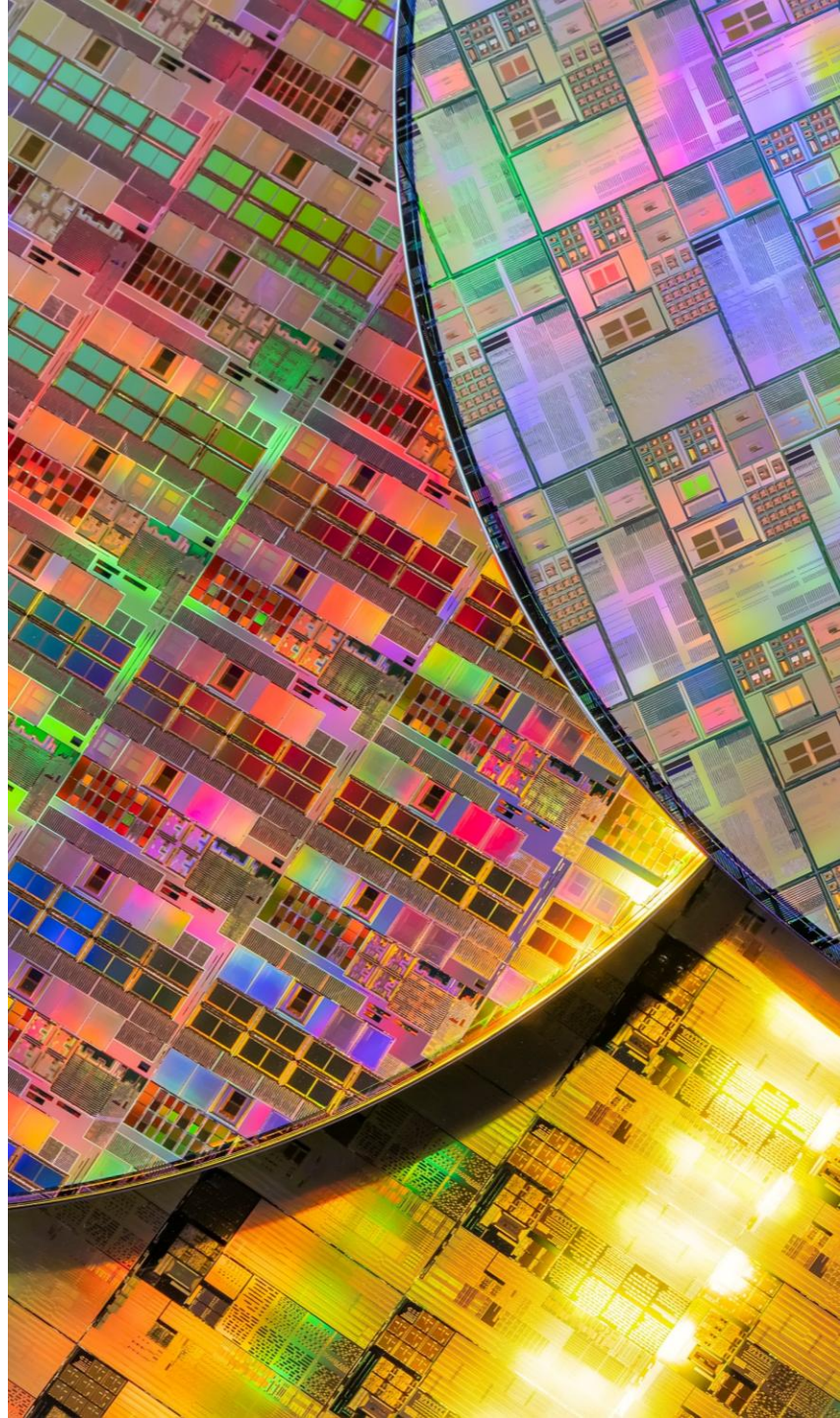
Previously

- Discovered tri-state drivers and high-impedance, for building busses
- Used behavioral modeling approach to describe logic circuits
- Verilog, continued
  - Always block
  - If-else statements
  - Switch statements

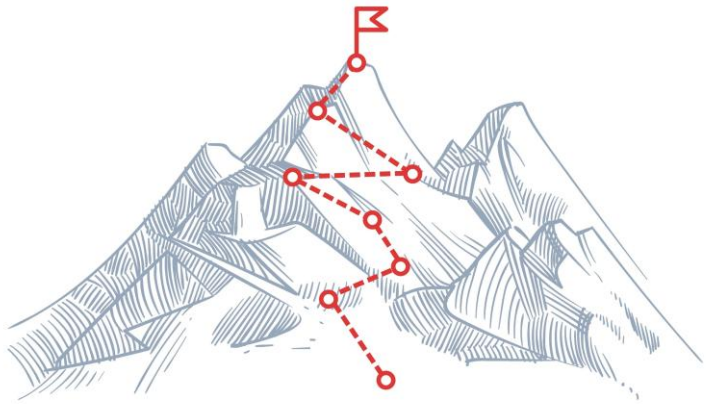


Let’s Talk About…

…transistors, CMOS gates,
real gate behavior, dynamic operation,
power consumption



Learning Outcomes



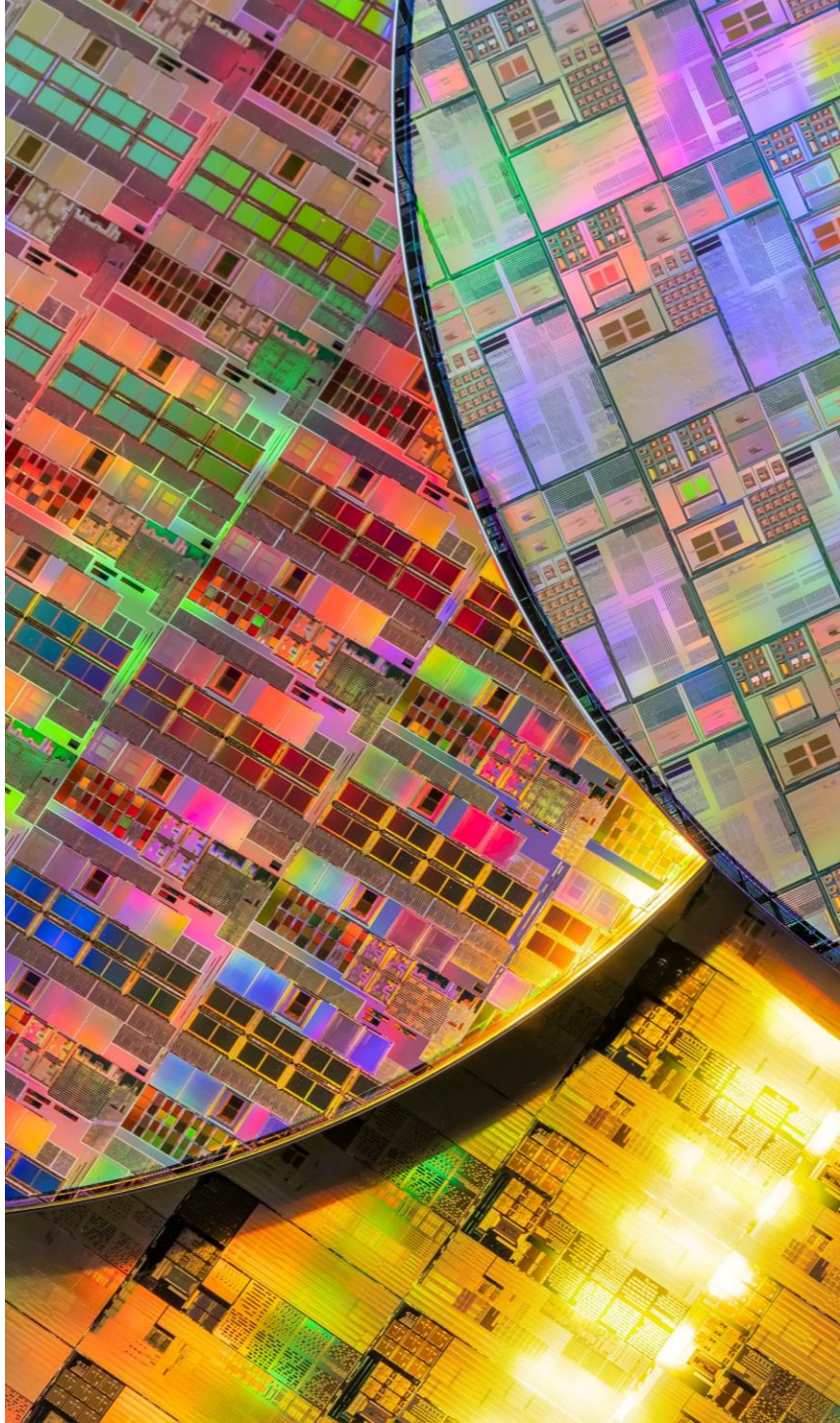
- Discover transistors, the basic components from which real logic gates are built
  - Complementary Metal-Oxide-Semiconductor (**CMOS**) technology
- Understand the difference between **ideal and real gate** behavior
  - Real gate **delays**: the time it takes for the output to reach logic values 0 or 1
- Be aware of the existence of **hazards** in real circuits to understand and avoid unwanted behavior when building complex logic circuits
- Learn which factors impact the working **frequency** and the **dynamic power** consumption of a logic circuit, and in what way

Quick Outline

- Transistors
  - NMOS
  - PMOS
  - CMOS
- Real Voltage Waveforms
  - Voltage transfer characteristic
  - Rise time and fall time
  - Propagation delay
- Dynamic operation
  - Fan-in and fan-out
  - Parasitic capacitance
  - Gate delay
  - Power dissipation
- Hazards
- Executive summary

Transistors

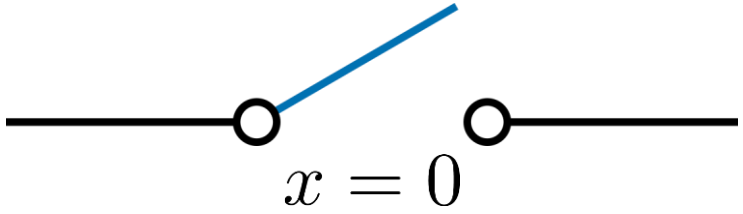
NMOS, PMOS, Complementary MOS (CMOS)



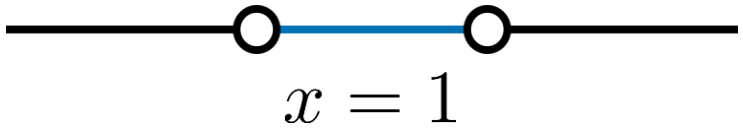
Transistor Switches – NMOS

Metal-Oxide-Semiconductor (MOS)

- If controlled by an input variable x, the switch is
  - Open if $x = 0$



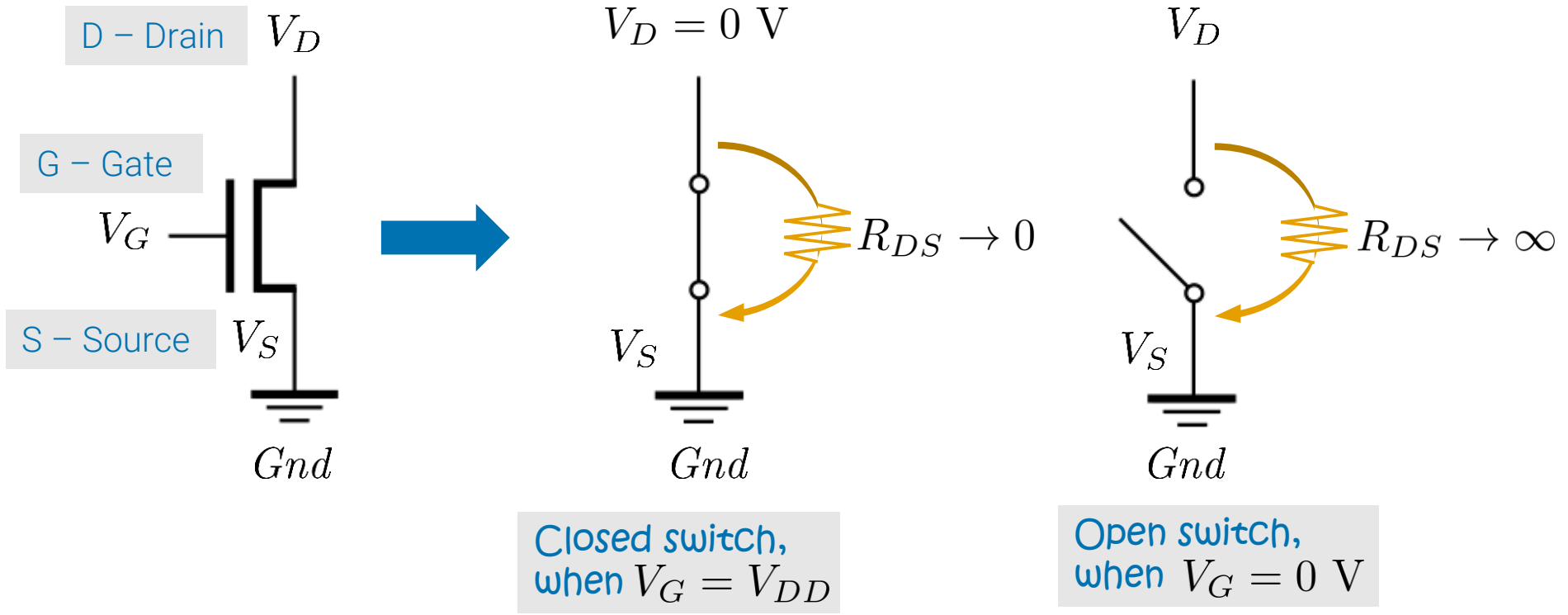
  - Closed if $x = 1$



Transistor Switches – NMOS

Metal-Oxide-Semiconductor (MOS)

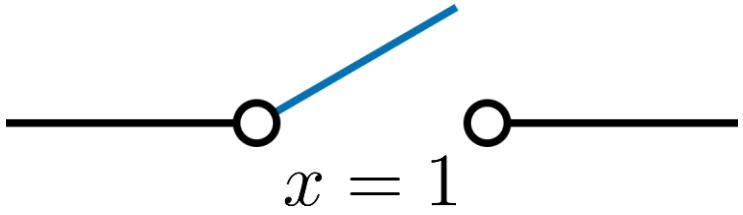
- NMOS as a logic gate



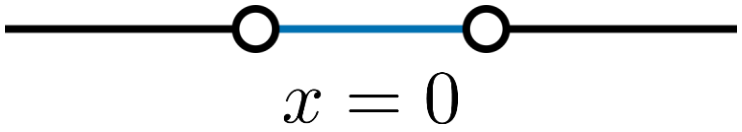
Transistor Switches – PMOS

Metal-Oxide-Semiconductor (MOS)

- If controlled by an input variable x, the switch is
  - Open if $x = 1$



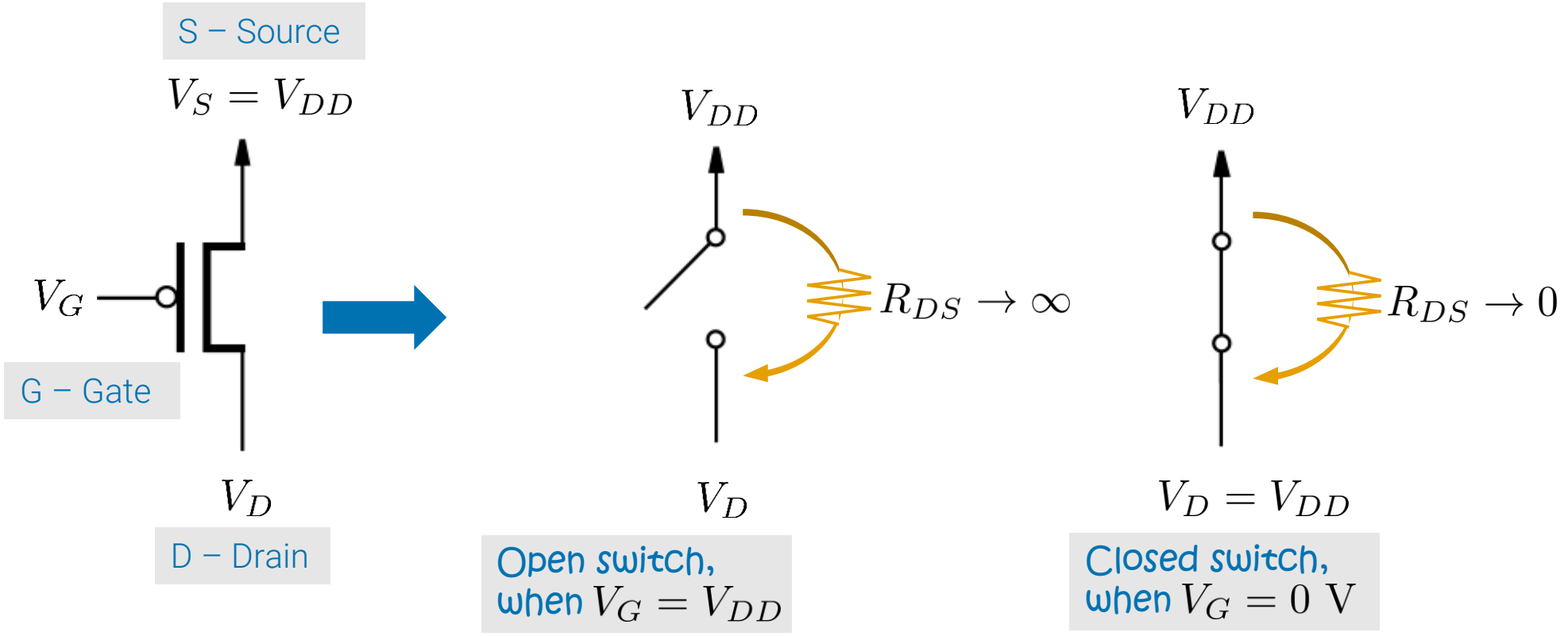
  - Closed if $x = 0$



Transistor Switches – PMOS

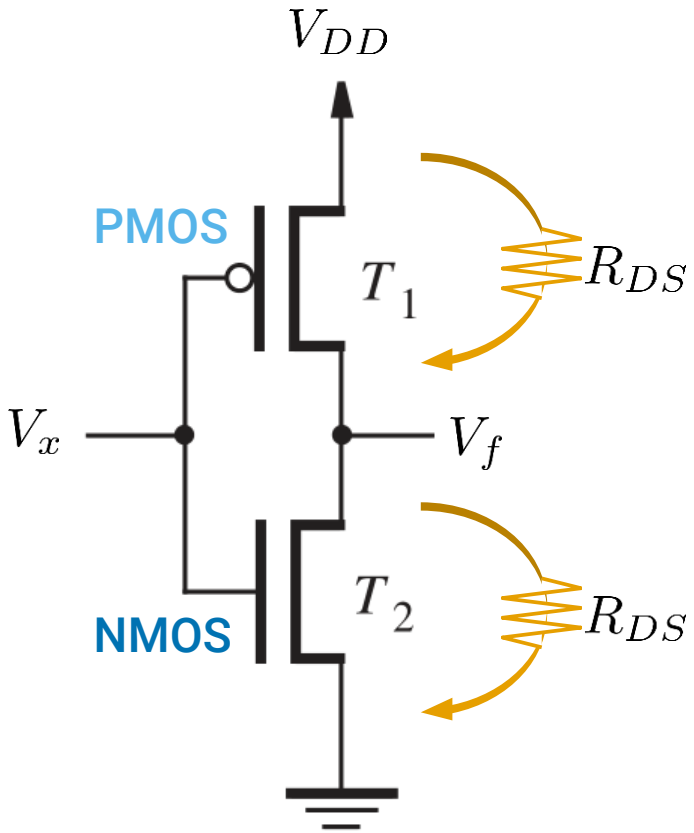
Metal-Oxide-Semiconductor (MOS)

- PMOS as a logic gate



Complementary MOS – CMOS

- PMOS and NMOS combined



- Truth table

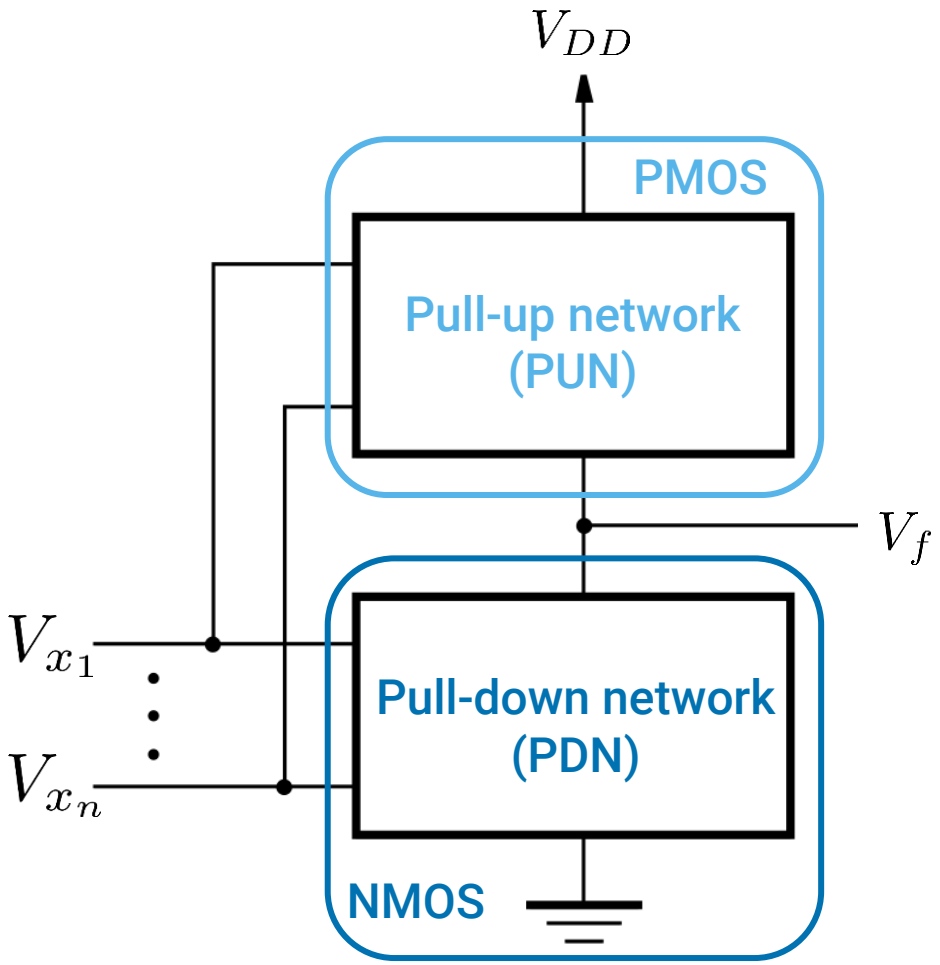
V_x	T_1	T_2	V_f
Gnd	ON	OFF	V_{DD}
V_{DD}	OFF	ON	Gnd

x	T_1	T_2	f
0	ON	OFF	1
1	OFF	ON	0

- This circuit is a **NOT gate**

CMOS Circuit Structure

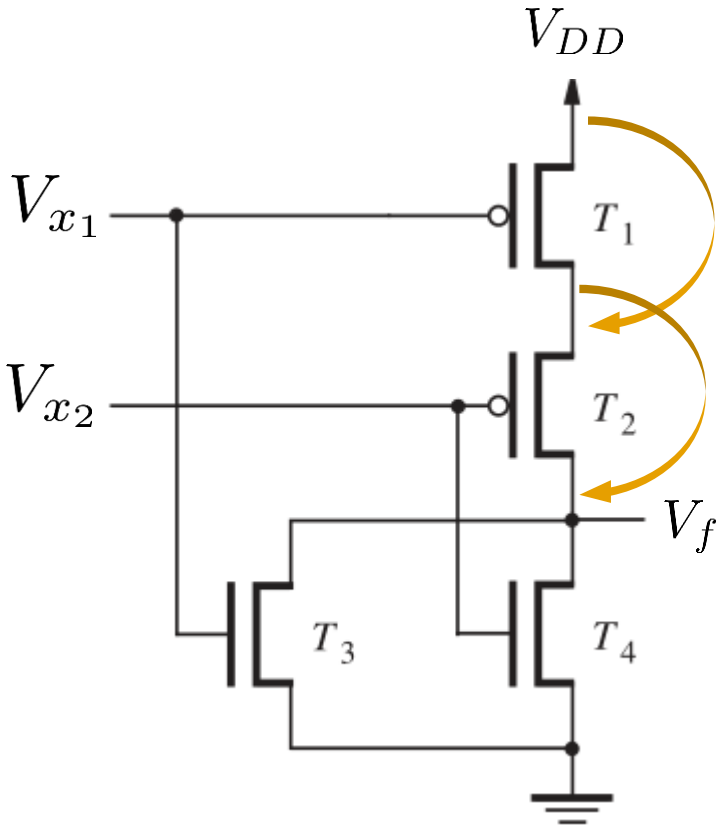
N inputs, single output



- **Complementary** functions performed by a pull-up and pull-down network:
  - **Pull-up** composed of **PMOS**
  - **Pull-down** composed of **NMOS**
- Pull-up and pull-down networks are **dual** to one another and have an **equal** number of transistors

CMOS Gates

- Find the functionality of the given CMOS gate



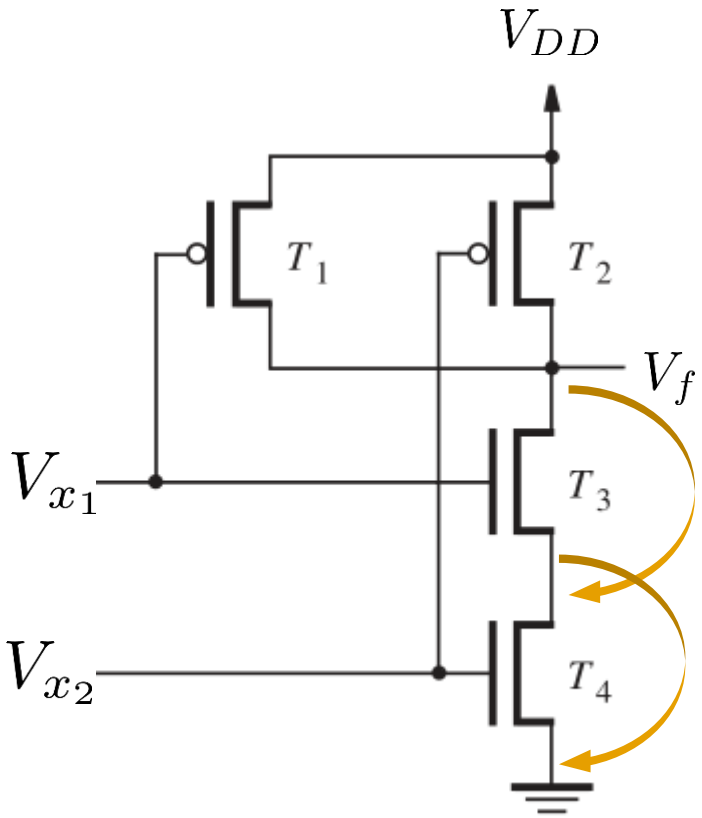
- Truth table

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

- Answer: NOR gate
- Cost (size, area): four transistors

CMOS Gates

- Find the functionality of the given CMOS gate



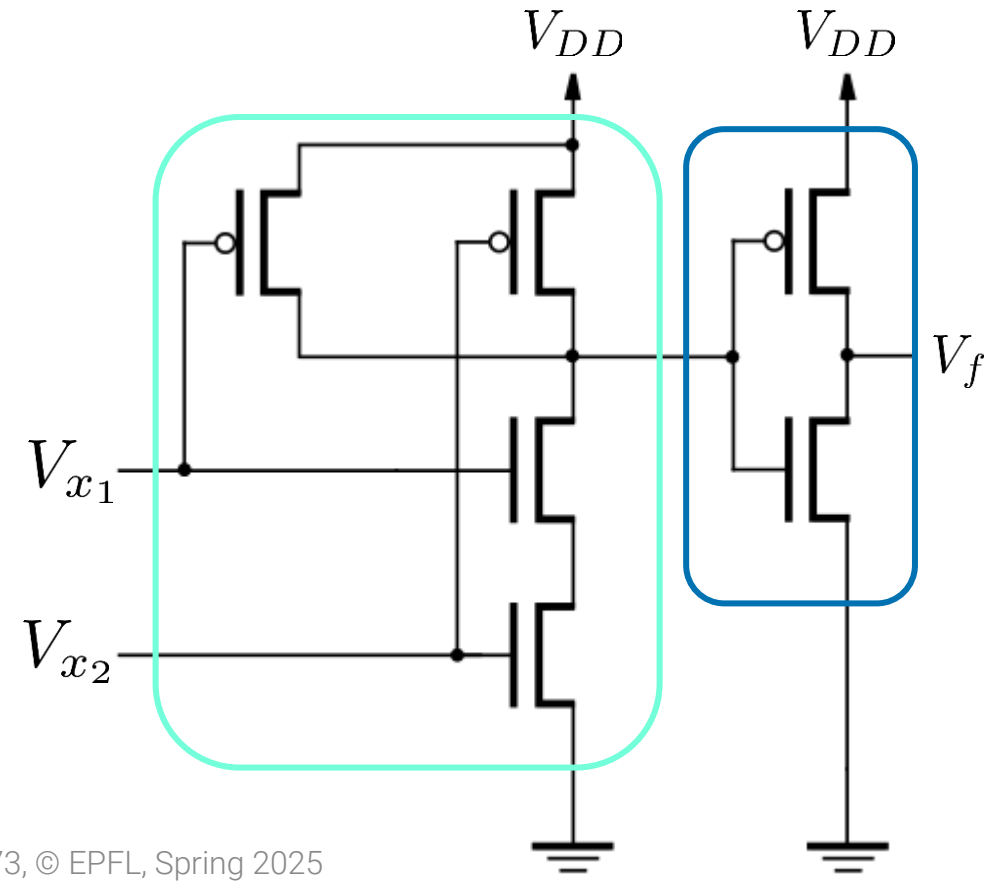
- Truth table

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

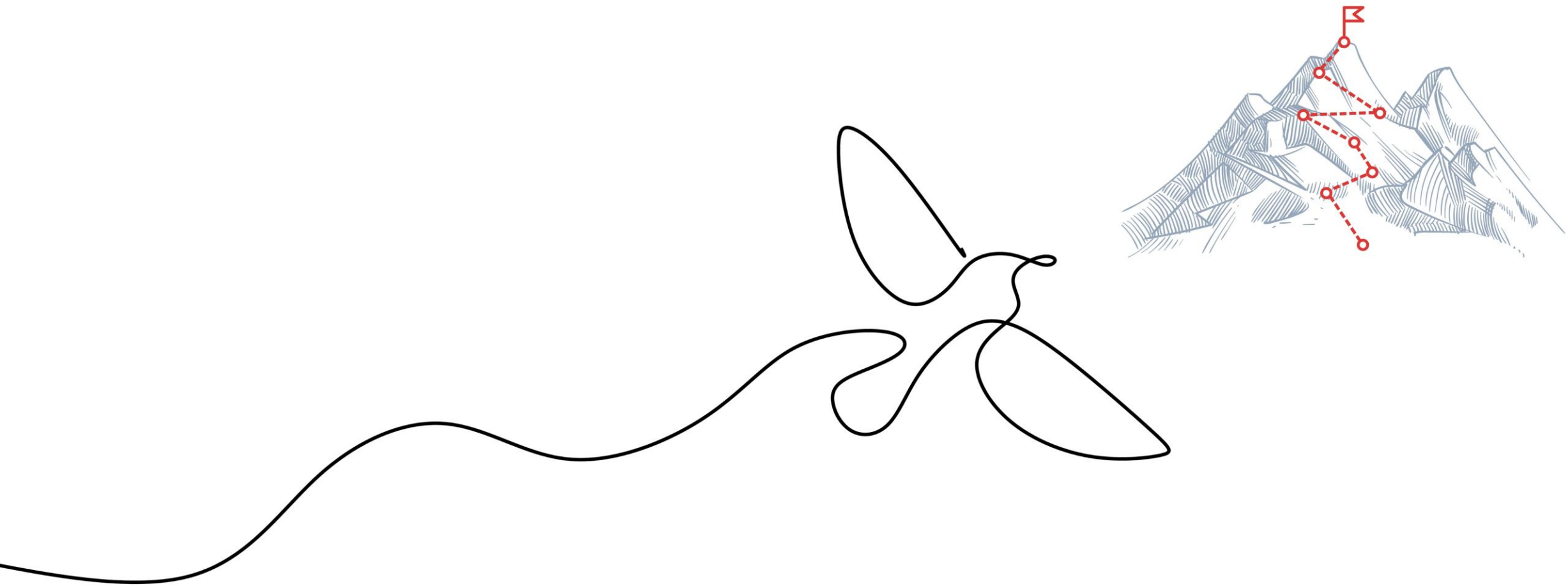
- Answer: NAND gate
- Cost (size, area): four transistors

CMOS Gates

- Find the functionality of the given CMOS gate

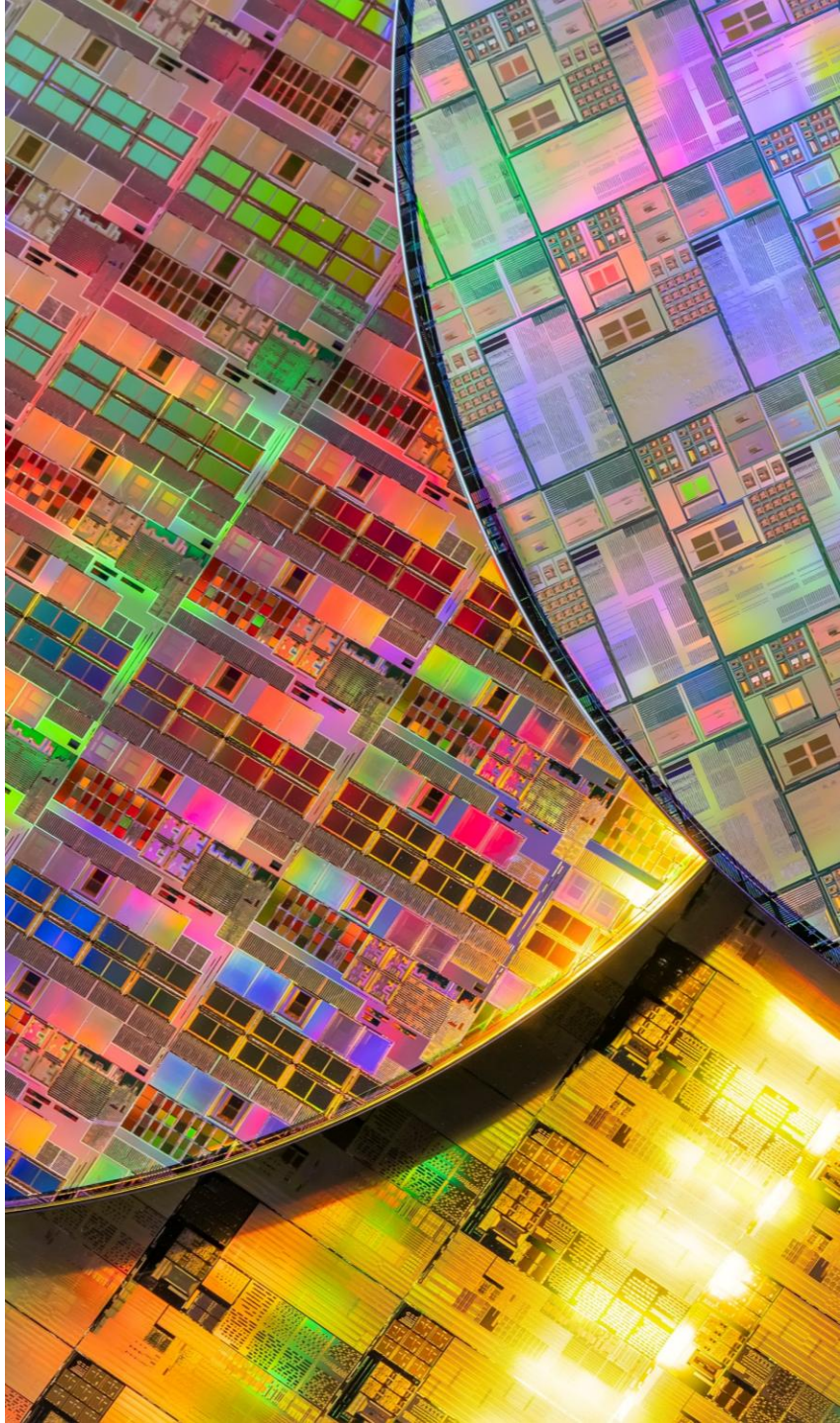


- NAND gate followed by a NOT gives us an AND gate
- Cost (size, area): six transistors, two more than the NAND gate



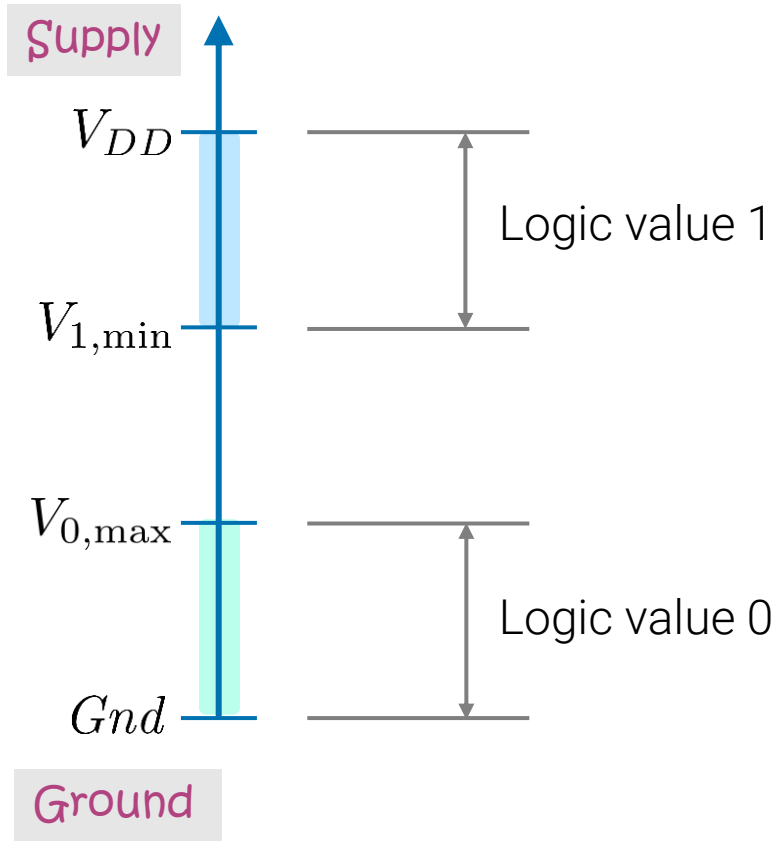
Real Voltage Waveforms

- Voltage transfer characteristic
- Rise and fall time
- Propagation delay



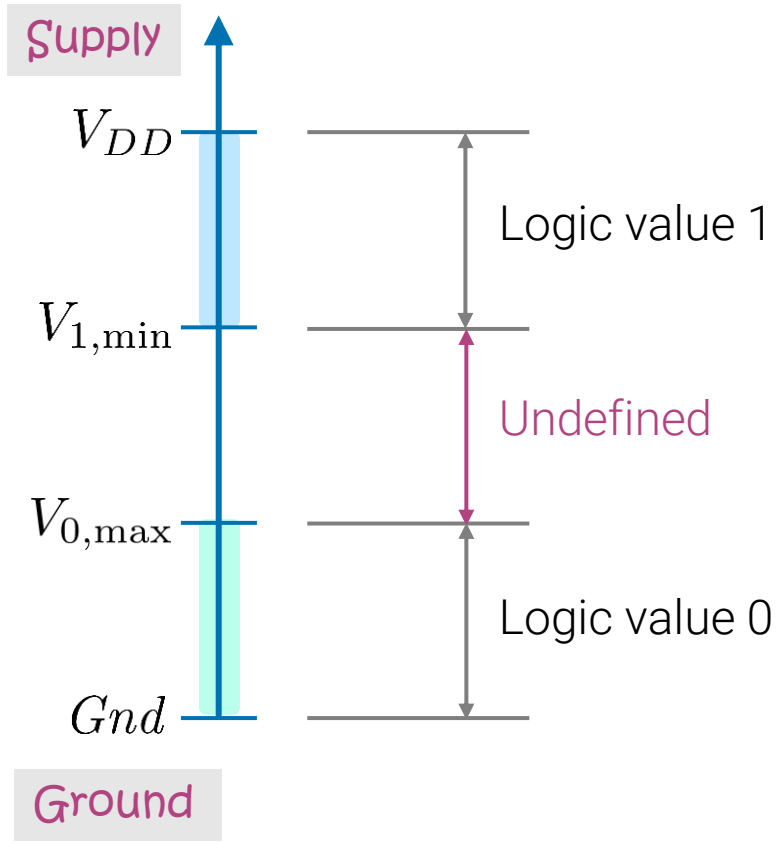
Logic Values as Voltage Levels

- Binary values (0, 1) in digital circuits are represented as voltage levels
  - **0: low** (ground)
  - **1: high** (supply)
- Thresholds:
  - $V_{0,\max}$ the **max** voltage level that the circuit must interpret as **low**
  - $V_{1,\min}$ the **min** voltage level that the circuit must interpret as **high**



Logic Values as Voltage Levels

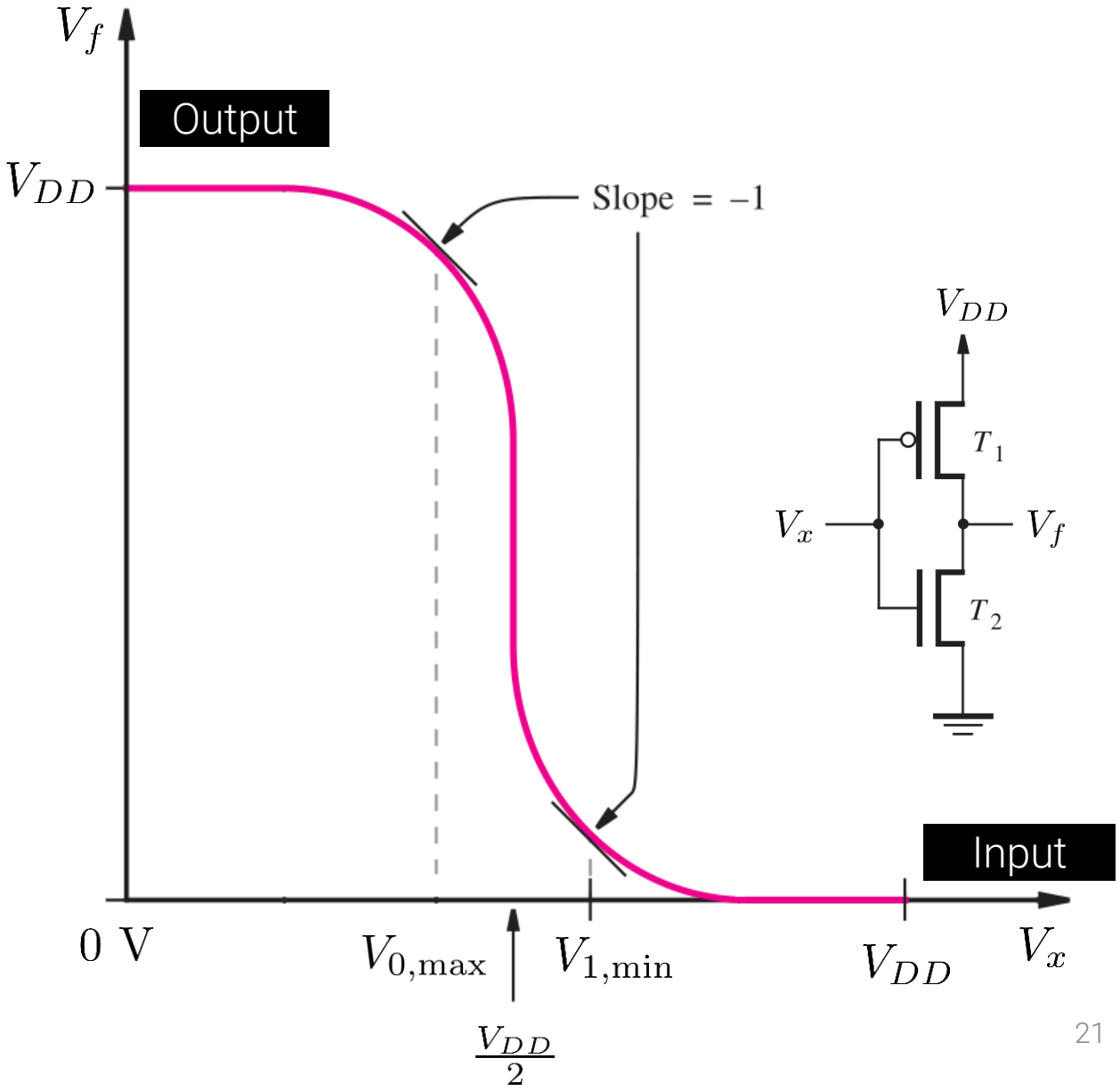
- Exact threshold values depend on the technology; typically:
  - $V_{0,\max} \sim 0.4 V_{DD}$
  - $V_{1,\min} \sim 0.6 V_{DD}$
- Range $(V_{0,\max}, V_{1,\min})$ is undefined
  - Logic signals take those intermediate voltage values only while transitioning from one logic value to another



Voltage Transfer Characteristic

CMOS Inverter (NOT Gate)

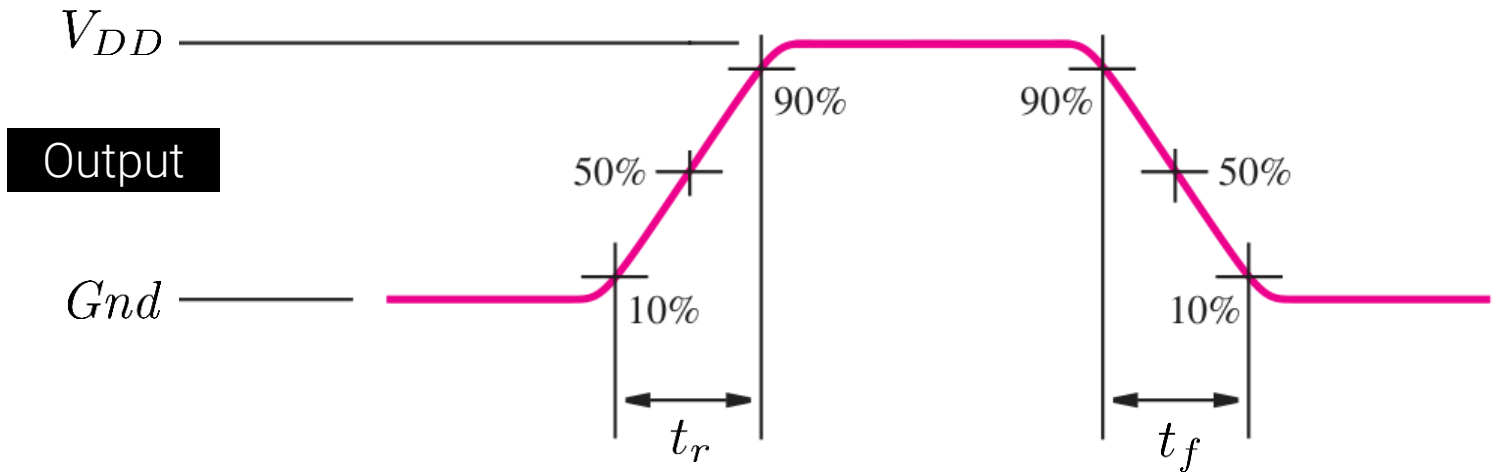
- The input-output voltage relationship in a real CMOS inverter is summarized by the voltage transfer characteristic
- Where the slope of the curve is -1, we have:
  - max input voltage that will be interpreted as low
  - min input voltage that will be interpreted as high



Real Voltage Waveforms for Logic Gates

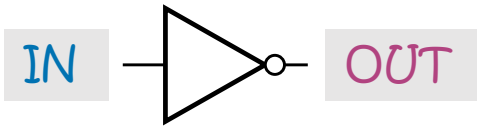
Rise Time, Fall Time

- Consider a logic gate **output** changing from one logic level to another. We used to draw an ideal (instantaneous) transition. In **real circuits**, waveforms do not have the ideal shape; instead, transitions take some time:
  - t_r, **rise time**, the time elapsed from $0.1V_{DD}$ to $0.9V_{DD}$
  - t_f, **fall time**, the time elapsed from $0.9V_{DD}$ to $0.1V_{DD}$

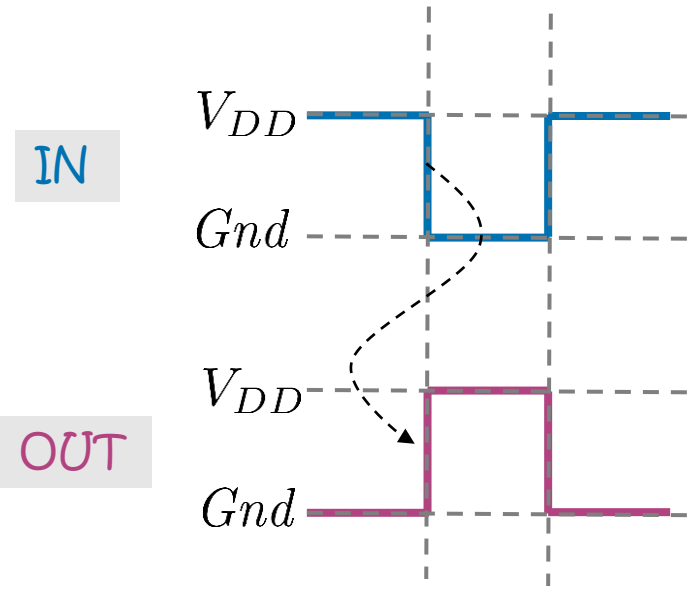


Voltage Waveforms for Logic Gates

- Consider a NOT gate driven by a voltage pulse.



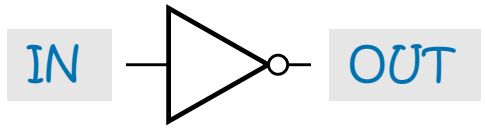
- Idealized in-out waveforms would be drawn like this. What is wrong here?



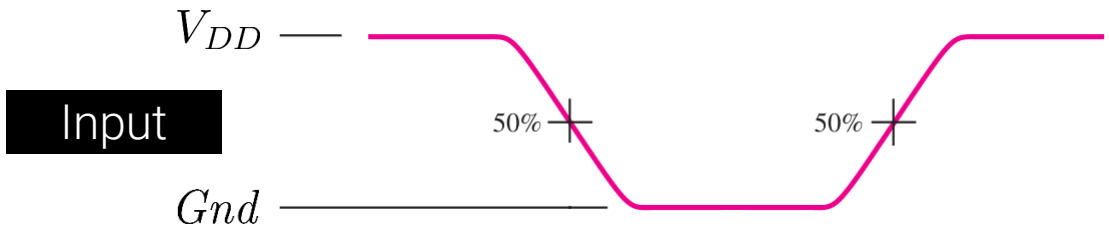
- **A**: First, in real gates, as we saw, the transitions are not ideal; they take time. Second, the time it takes for a signal to propagate from the input to the output is not null. There is a **propagation delay**.

Real Voltage Waveforms for Logic Gates

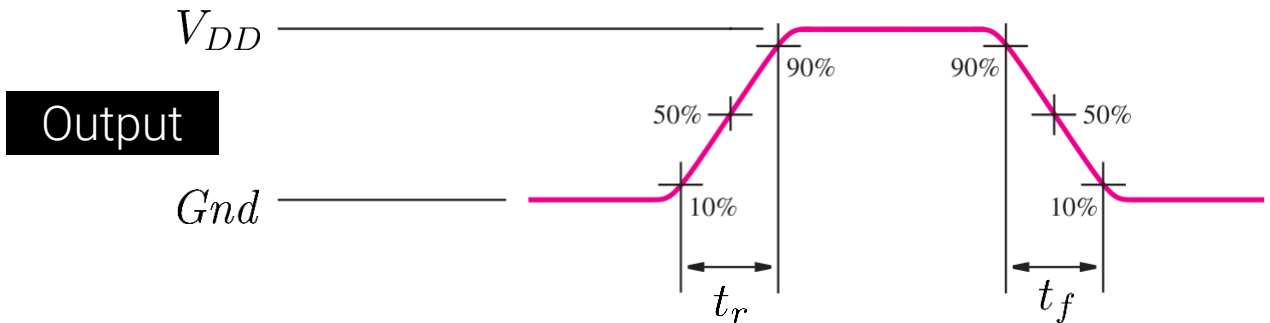
- Consider a NOT gate driven by a voltage pulse



- Real-looking input waveform would be, for example:



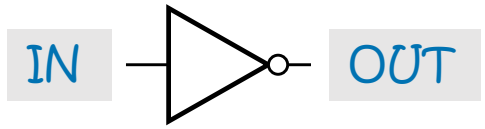
- The corresponding real-looking output waveform:



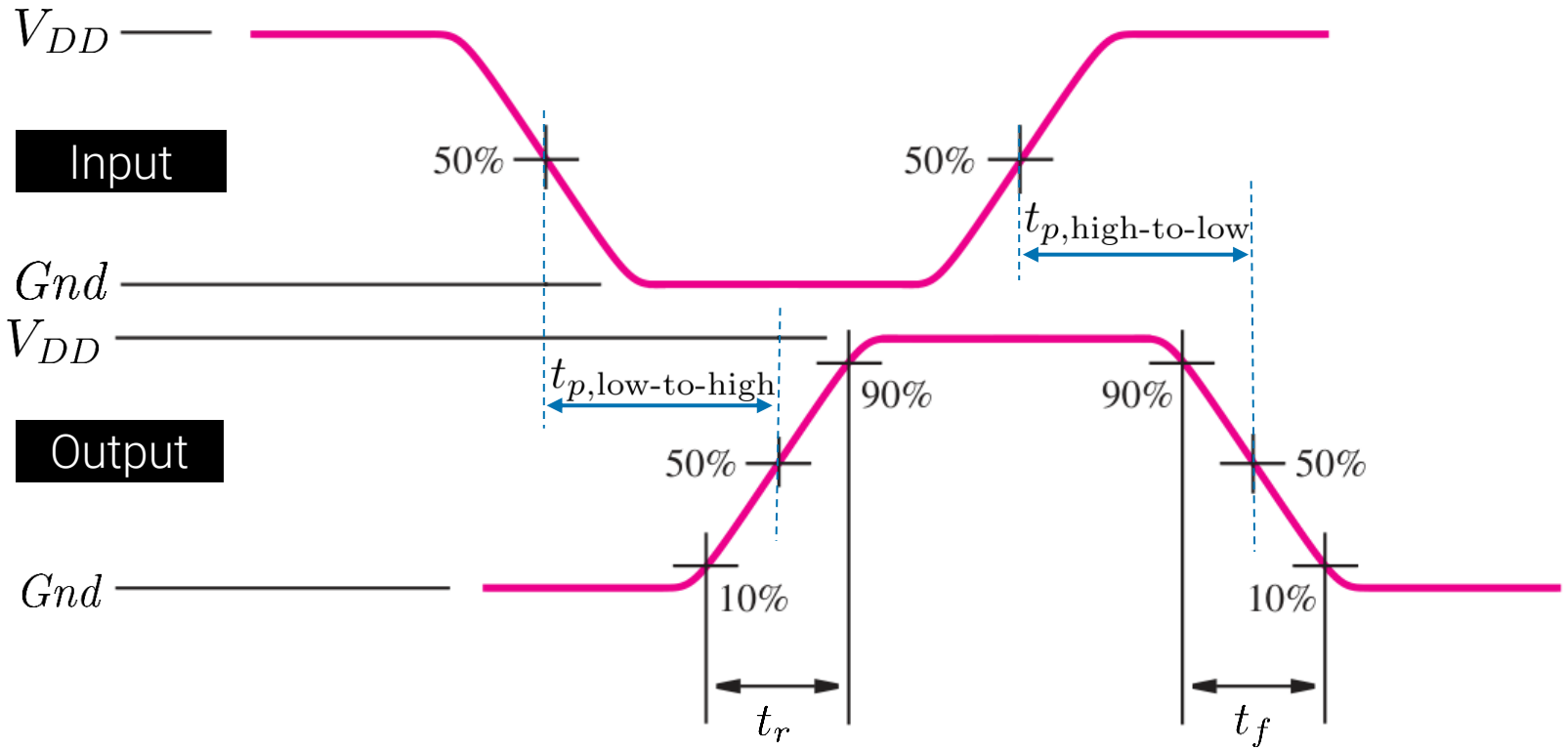
Real Voltage Waveforms for Logic Gates

Propagation Delay

- Consider a NOT gate driven by a voltage pulse



- After aligning the waveforms in time, we see the propagation delay

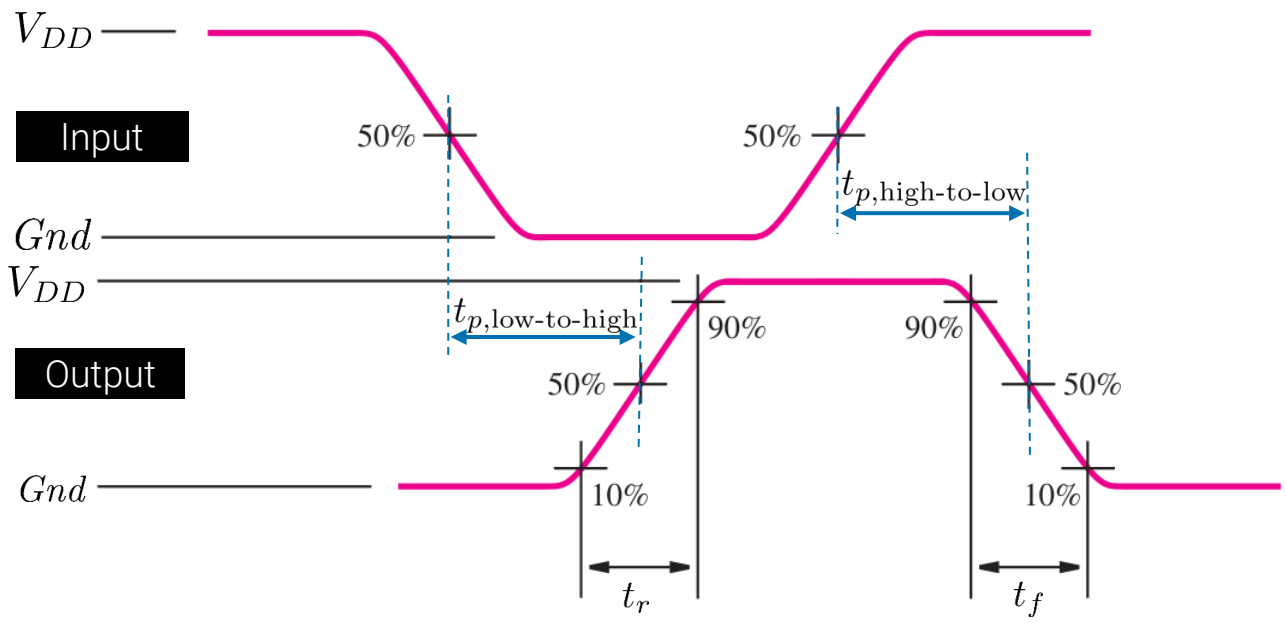


Real Voltage Waveforms for Logic Gates

Propagation Delay, Contd.

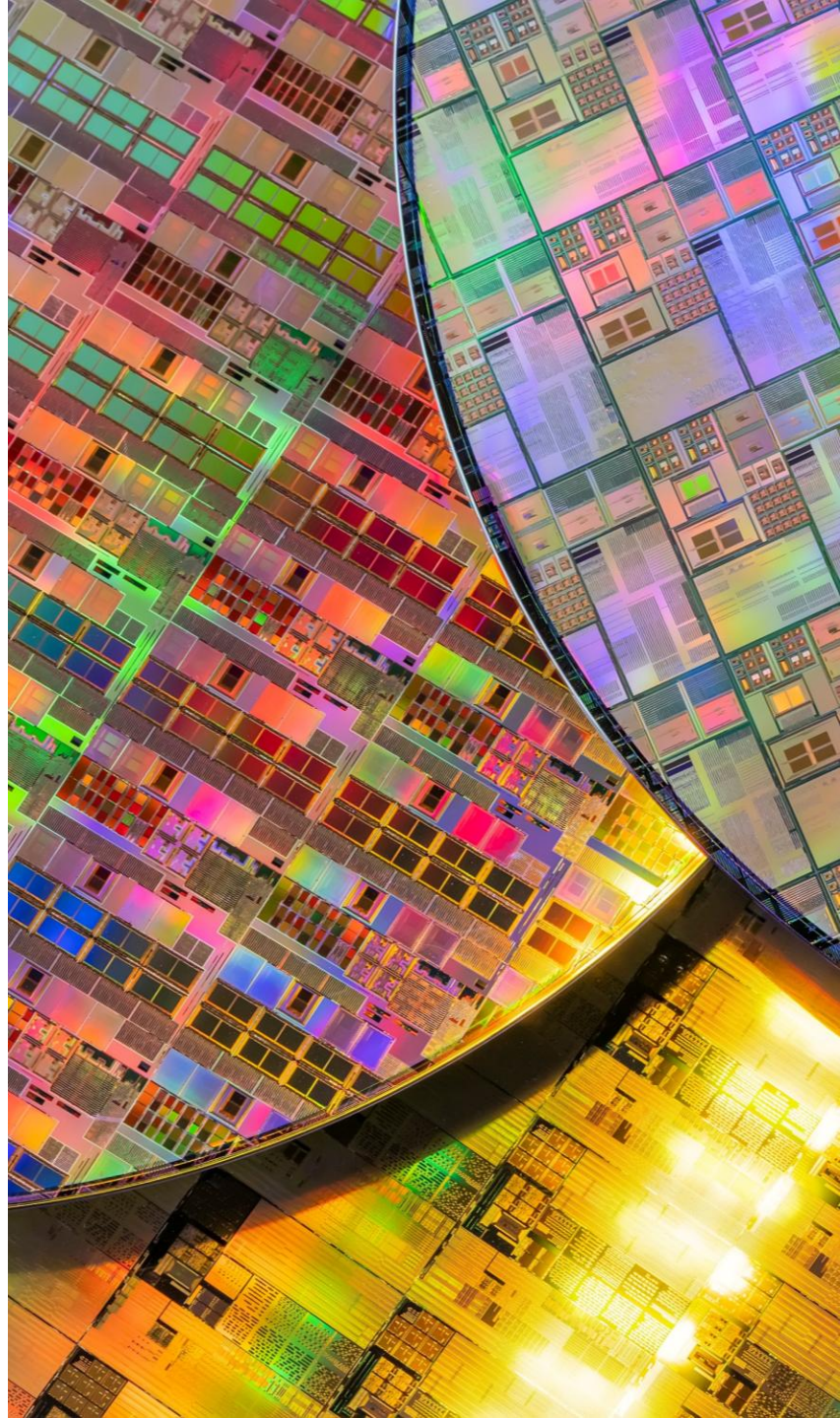
- Propagation delay, t_p, is the time from when the input voltage reaches 50% of the V_{DD}, to the time the output voltage reaches the same level
- General case:

$$t_{p,\text{high-to-low}} \neq t_{p,\text{low-to-high}}$$



Dynamic Operation

…and Power Dissipation



Fan-In of a Logic Gate

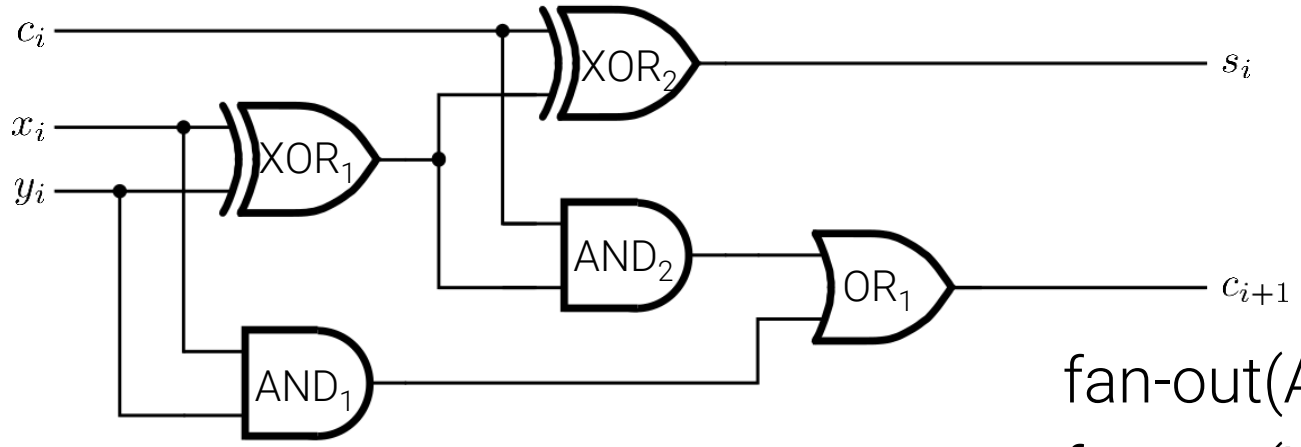
Definitions

- **Fan-in** of a logic gate is the number of its inputs
- Examples
  - NOT has a fan-in of one
  - tree-input NOR gate has a fan-in of three
  - four-input XOR gate has a fan-in of four

Fan-Out of a Logic Gate

Definitions

- **Fan-out** of a logic gate is the number of other gate inputs it drives (i.e., “the load”)
- Example



fan-out(AND$_1$) = fan-out(AND$_2$) = 1

fan-out(XOR$_1$) = **2**;

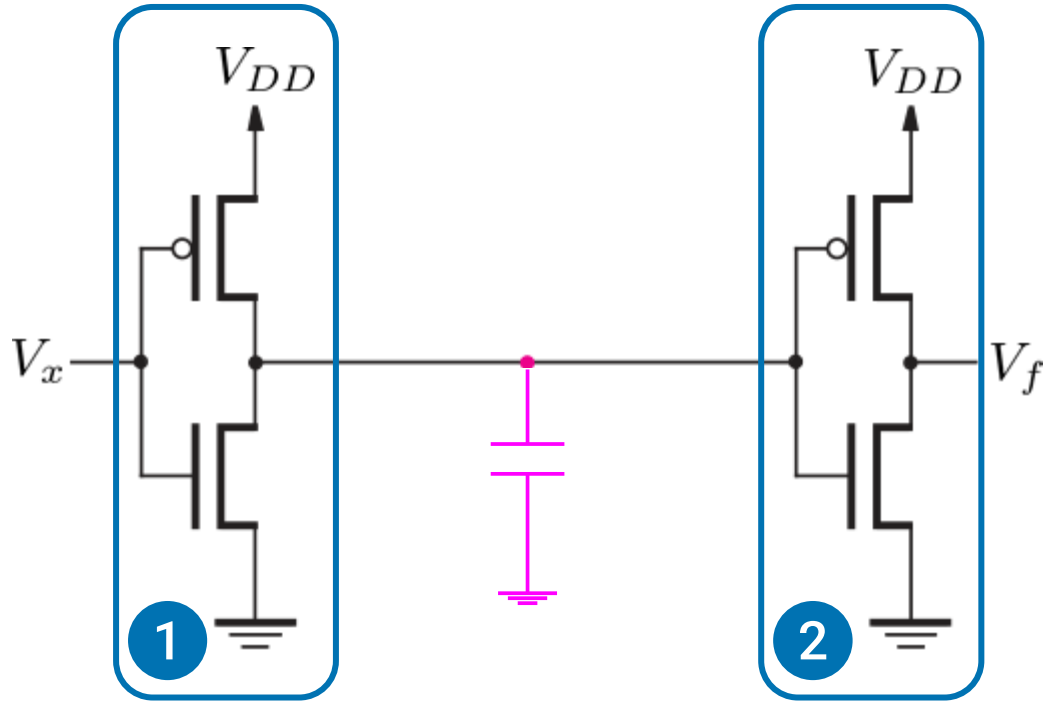
fan-out(XOR$_2$) = ? (not shown)

fan-out(OR$_1$) = ? (not shown)

Parasitic Capacitance

Impact of Fan-out on Gate Delay

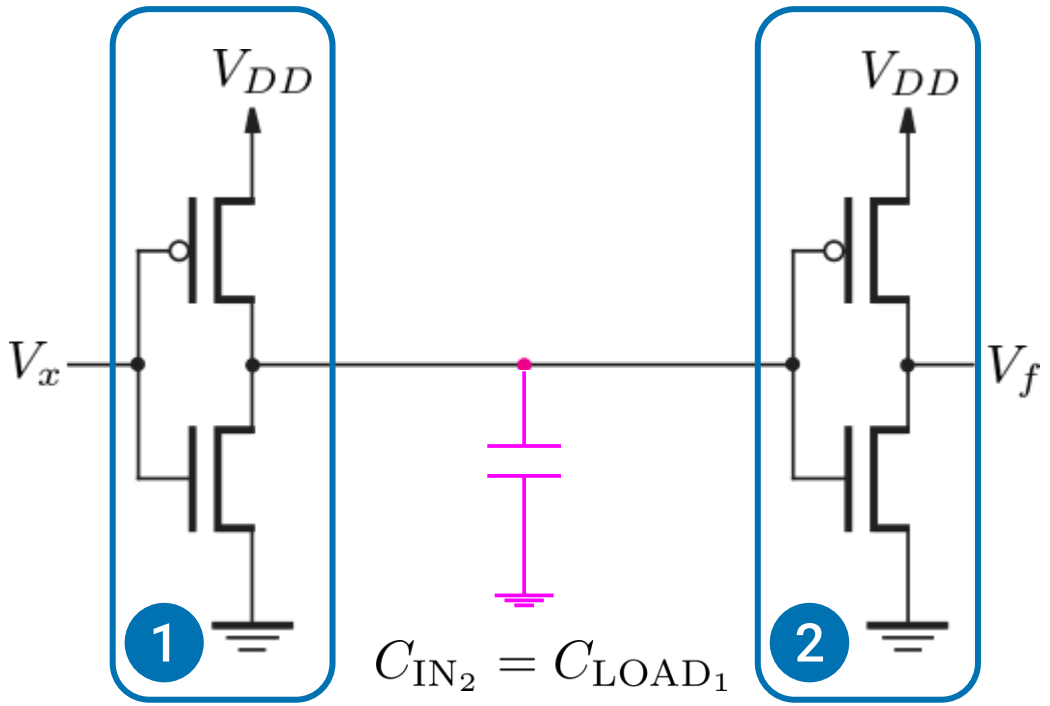
- An undesired but unavoidable side-effect of transistor fabrication is the **input** **parasitic capacitance** of a logic gate



Parasitic Capacitance

Impact of Fan-out on Gate Delay

- The **sum** of all **transistor gate terminal capacitances** at an input of a logic gate gives the equivalent per-input capacitance of that logic gate
  - Per-input capacitance acts as a "load" to the logic gate that drives this input
  - Example in the figure: input capacitance of the 2nd NOT gate acts as "load" at the output of the 1st NOT gate

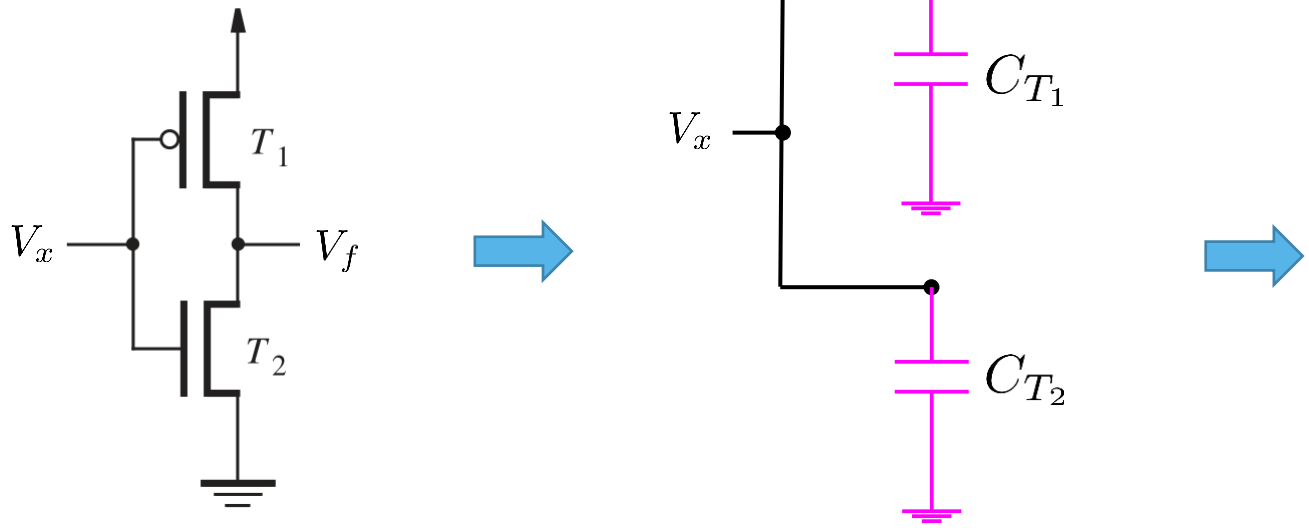


**The higher the load capacitance, the slower the gate whose output is connected to it*

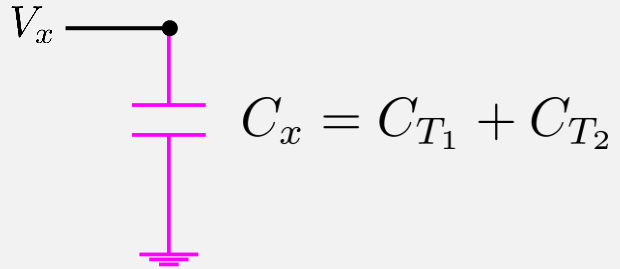
Gate Input Capacitance

NOT Gate

- Given the NMOS/PMOS transistor gate capacitance C_T, find the input capacitance of a NOT gate
- Solution: identify all transistors connected to the NOT gate input; sum their gate capacitances to find the equivalent per-input C of the NOT gate



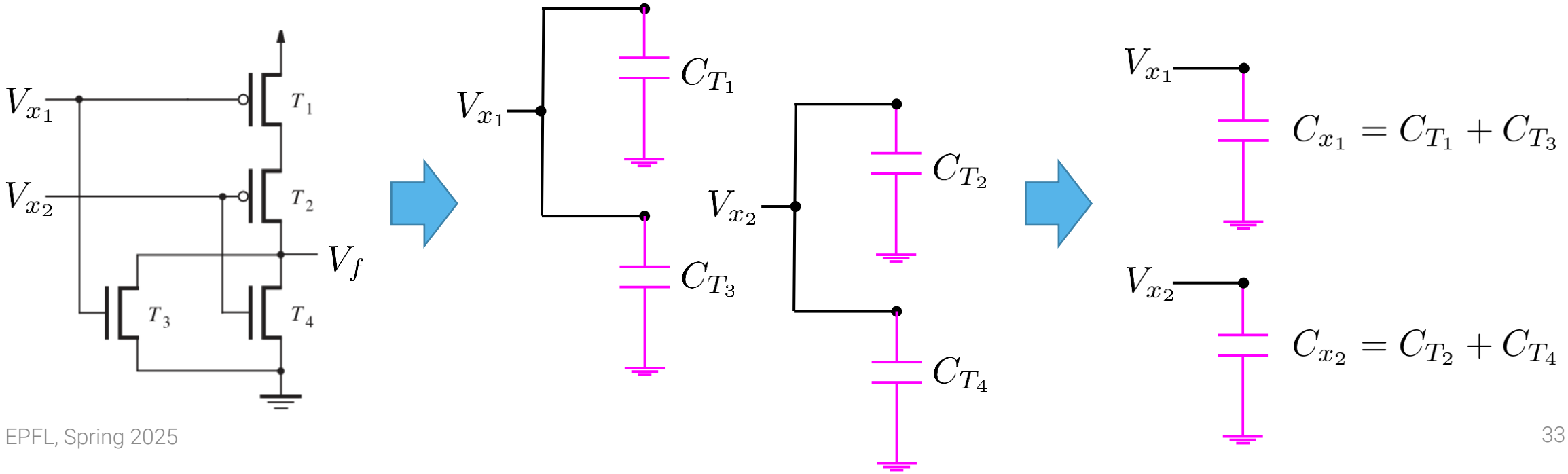
Equivalent capacitance of two or more capacitors connected **in parallel** is the **sum** of their individual capacitances [Read more online]



Gate Input Capacitance

NOR Gate

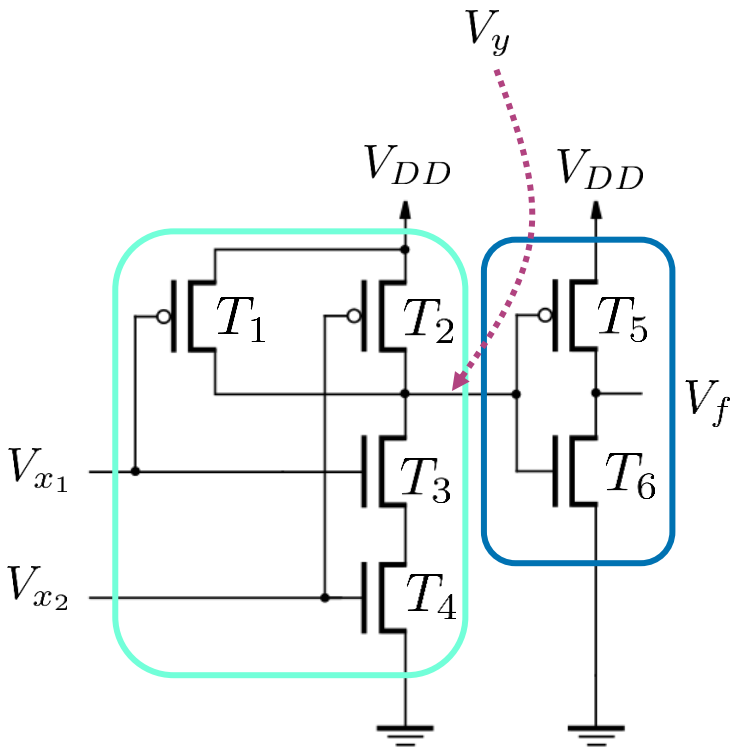
- Find the input capacitance of a NOR gate
- Solution: identify all transistors connected to the NOR gate inputs; sum their gate capacitances to find the equivalent per-input C of the NOR gate

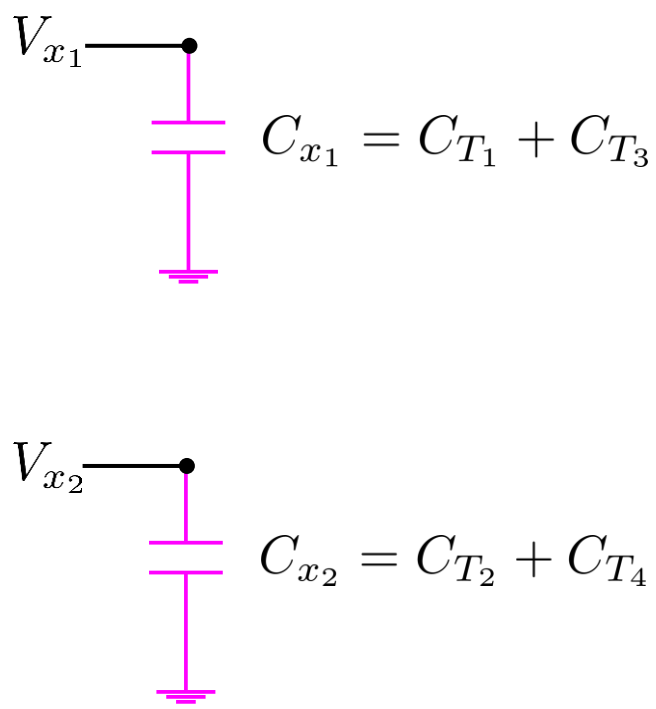


Gate Input Capacitance

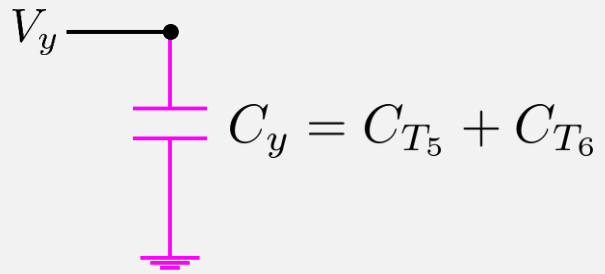
NAND followed by NOT

- Find the capacitance at terminals V_{x_1}, V_{x_2} and V_y



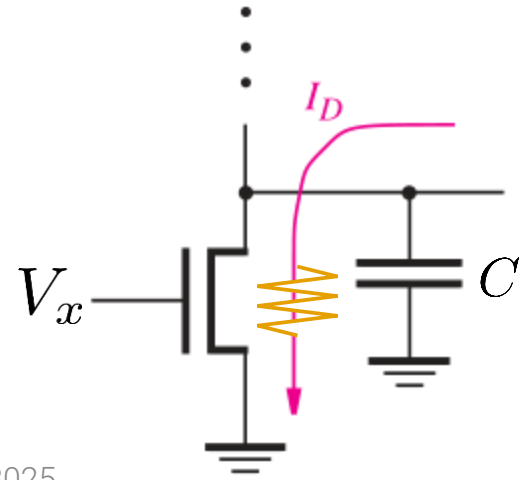


Input gate capacitance of the NOT gate acts as the **load capacitance** for the preceding NAND gate

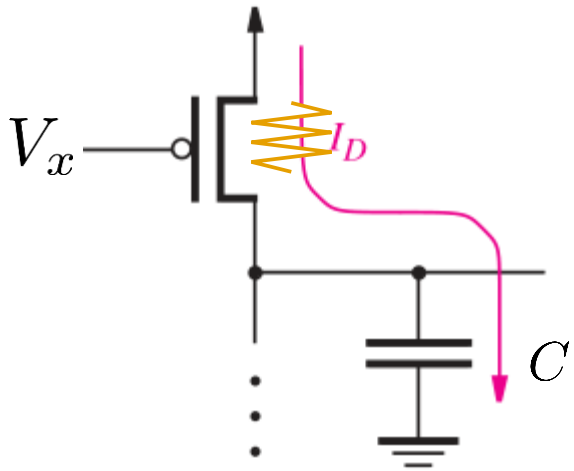


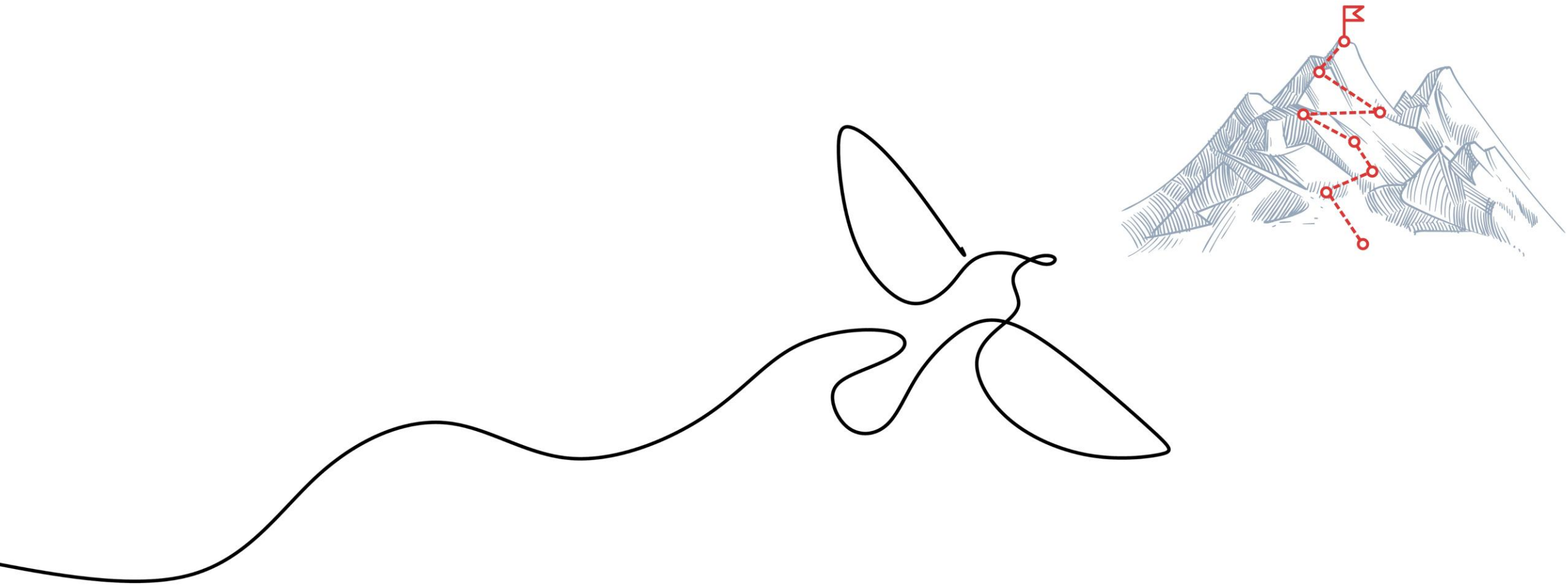
Dynamic Current Flow

- Current flow when input V_x changes: 0→V_{DD}
- Load capacitance is **discharged** through the NMOS on-resistance; PMOS is OFF

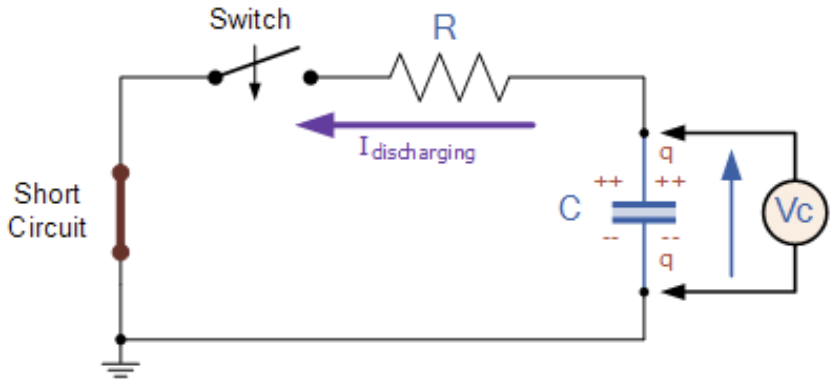


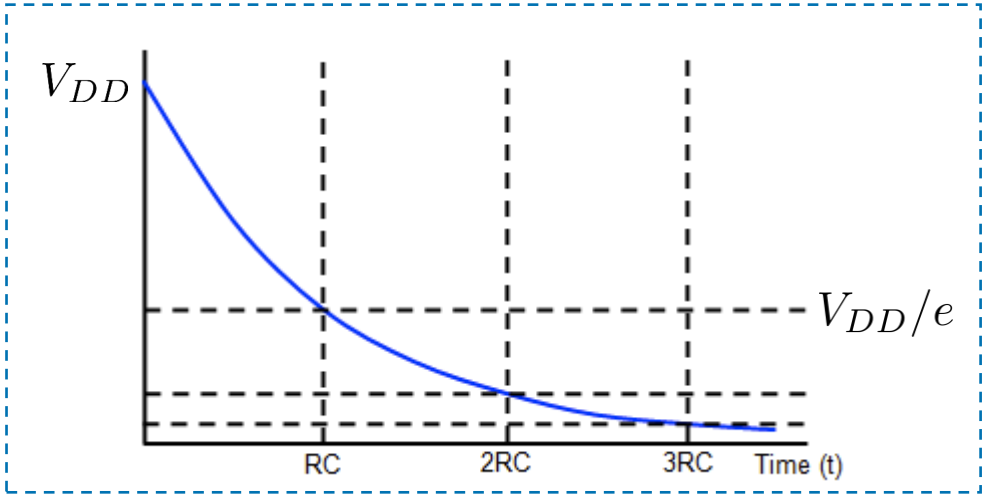
- Current flow when input V_x changes: V_{DD} → 0
- Load capacitance is **charged** through the PMOS on-resistance; NMOS is OFF





Discharging a Capacitor





- Kirchhoff's voltage law: the total voltage drop in a closed circuit is zero

$$V_c(t) - R \cdot i(t) = 0$$

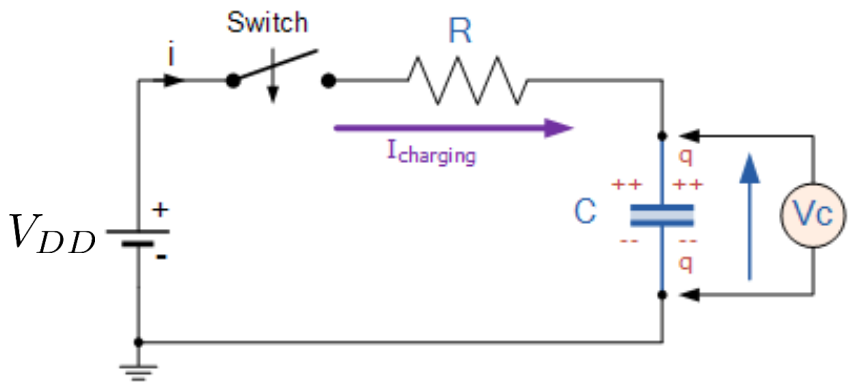
- Circuit current:

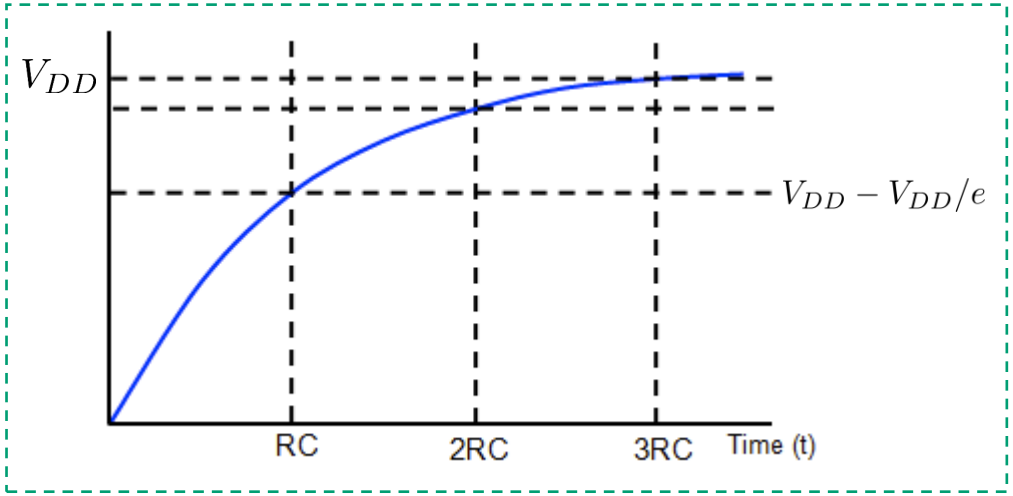
$$i(t) = i_R(t) = i_c(t) = C\frac{\mathrm{d}V_c(t)}{\mathrm{d}t}$$

- Assuming the initial capacitor voltage is V_{DD}, substituting the expression for the current and solving for the capacitor voltage brings us to

$$V_c(t) = V_{DD}e^{-\frac{t}{RC}}$$

Charging a Capacitor





- Kirchhoff's voltage law: the total voltage in a circuit is 0~V

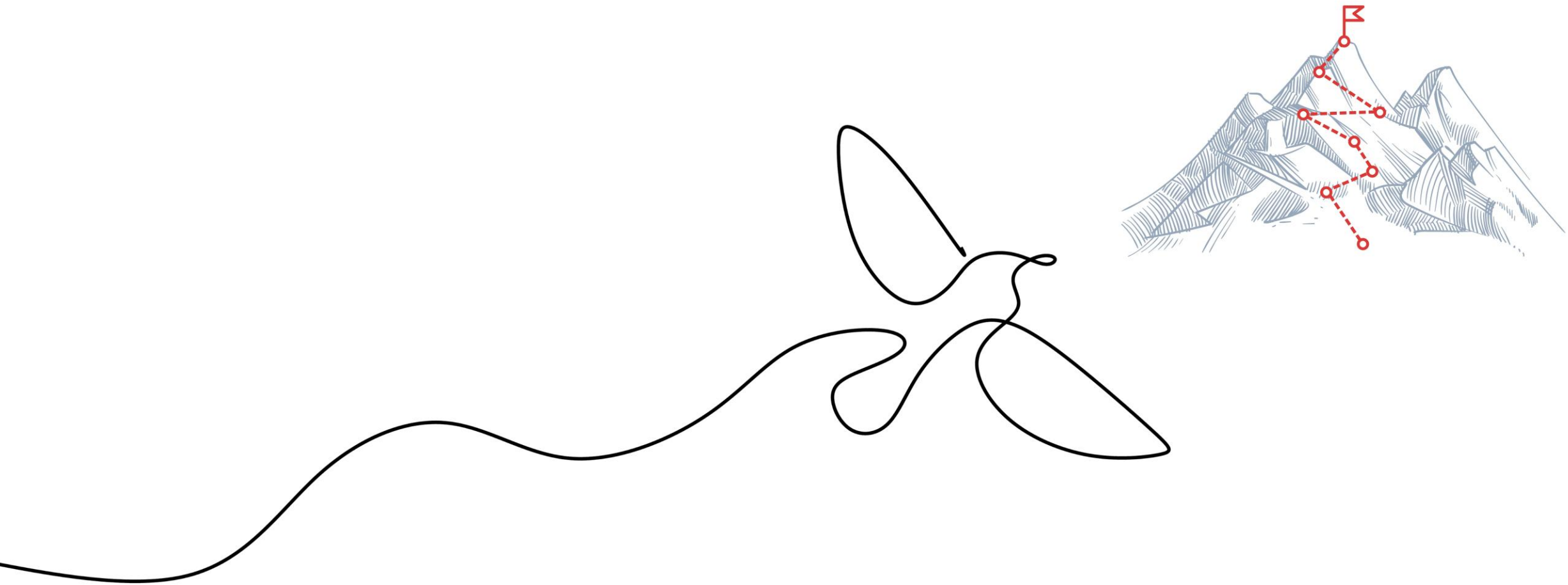
$$V_{DD} - R \cdot i(t) - V_c(t) = 0$$

- Circuit current:

$$i(t) = i_R(t) = i_c(t) = C\frac{\mathrm{d}V_c(t)}{\mathrm{d}t}$$

- Assuming the initial capacitor voltage was 0 V, substituting the expression for the current and solving for the capacitor voltage brings us to

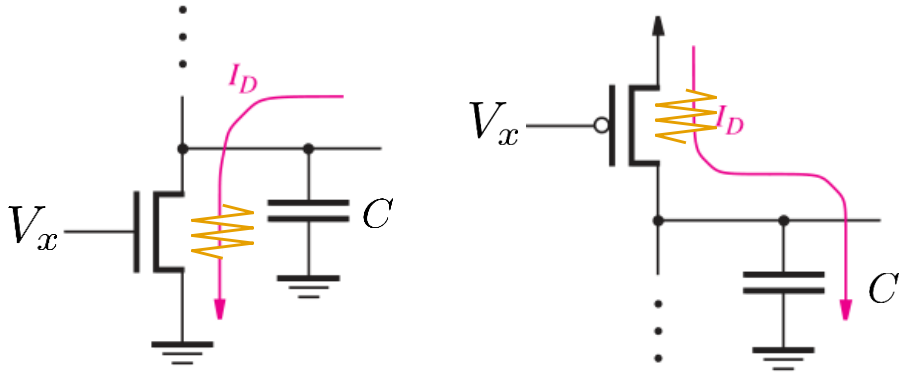
$$V_c(t) = V_{DD}(1 - e^{-\frac{t}{RC}})$$



The Speed of a Logic Circuit

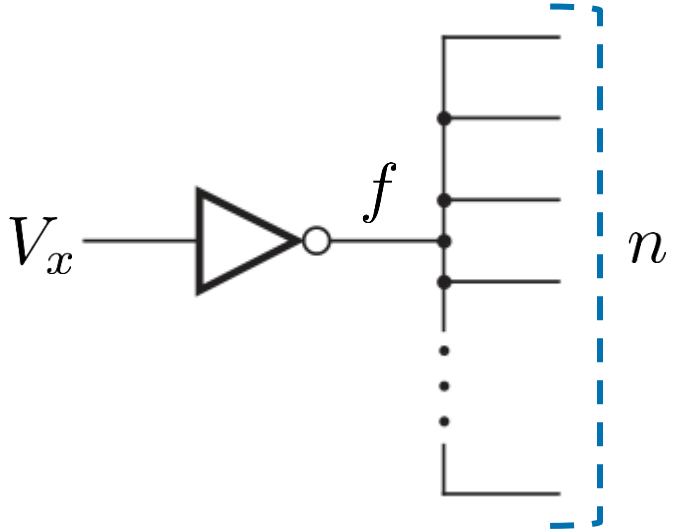
Gate Delay

- The speed (delay) depends on how fast the load capacitance is charged or discharged through the NMOS (PMOS) resistance R_{DS}
- **Fan-in and fan-out matter**
  - With higher fan-in grows the per-input capacitance
  - The higher the fan-out, the higher the equivalent load capacitance
- The **higher** the load **capacitance**, the **slower** the gate driving it



The Effect of Fan-Out on Gate Delay

- Consider the inverter with a fan-out n, which drives n other identical inverters. If the propagation delay of the inverter when $n = 1$ is $t_p = 0.2$ ns , find the propagation delay when $n = 5$



Load Capacitance Effect on Gate Delay

- Let us first see how much slower charging/discharging of a capacitor becomes with increased load capacitance
- Capacitor voltage while discharging (left) and charging (right) :

$$V_{C_1}(t) = V_{DD}e^{-\frac{t}{RC_1}}$$

$$V_{C_2}(t) = V_{DD}e^{-\frac{t}{RC_2}}$$

$$V_{low} = V_{DD}e^{-\frac{t_{1,low}}{RC_1}} = V_{DD}e^{-\frac{t_{2,low}}{RC_2}}$$

$$\frac{t_{1,discharge}}{RC_1} = \frac{t_{2,discharge}}{RC_2}$$

$$t_{2,discharge} = \frac{C_2}{C_1}\ t_{1,discharge}$$

$$V_{C_1}(t) = V_{DD}(1 - e^{-\frac{t}{RC_1}})$$

$$V_{C_2}(t) = V_{DD}(1 - e^{-\frac{t}{RC_2}})$$

$$V_{high} = V_{DD}(1 - e^{-\frac{t_{1,high}}{RC_1}}) = V_{DD}(1 - e^{-\frac{t_{2,high}}{RC_2}})$$

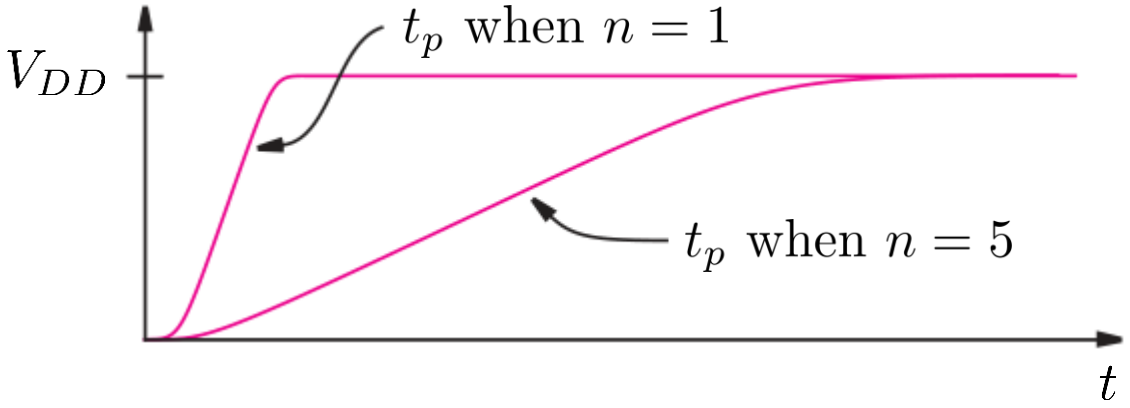
$$\frac{t_{1,charge}}{RC_1} = \frac{t_{2,charge}}{RC_2}$$

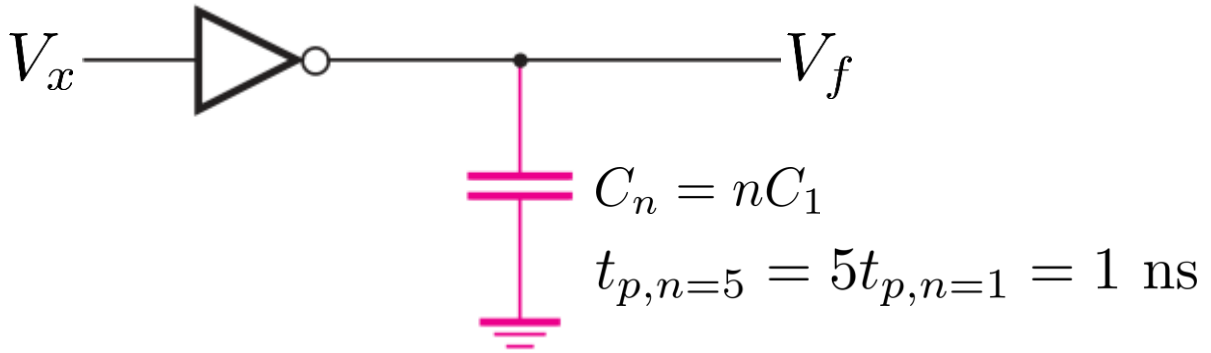
$$t_{2,charge} = \frac{C_2}{C_1}\ t_{1,charge}$$

- Therefore, increasing load capacitance leads to slower charge/discharge and, consequently, longer signal propagation time through the logic gate

The Effect of Fan-Out on Gate Delay

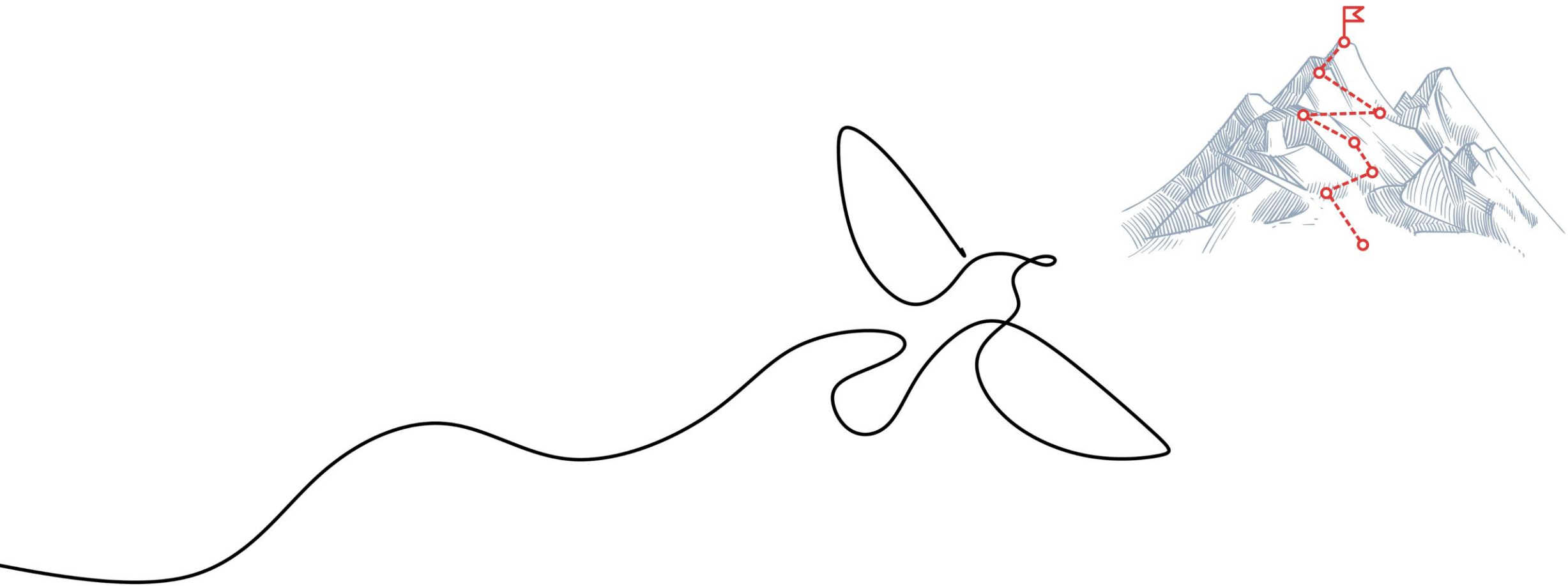
- Going back to our question…
- The capacitance at the output of the NOT gate is $nC_1 = 5C_1$





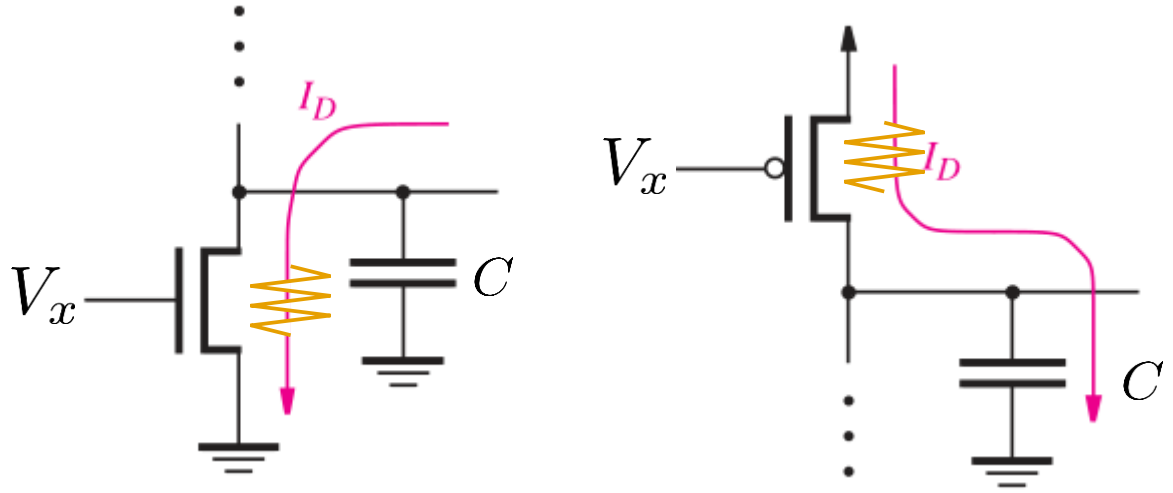
- Answer: NOT gate will be five times slower

Note: In reality, other parasitic components (capacitors, inductors, resistors) exist, and the expressions are more complex.



Power Dissipation in Logic Gates

- Power dissipation is an important consideration in all applications of logic circuits, especially in battery-operated devices
  - When NMOS is ON, the load capacitor discharges its energy
  - When PMOS is ON, the capacitor charges energy



Total Energy Stored in a Capacitor

- A capacitor C has been charged to the voltage $V_c = V_{DD}$
- Find the amount of energy stored in the capacitor

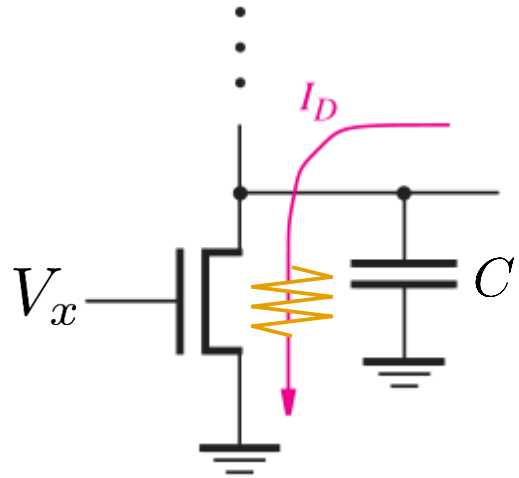
- Let us compute the energy that will be discharged instead:
  - Current flow through the capacitor: $i(t) = C\frac{\mathrm{d}V_c(t)}{\mathrm{d}t}$
  - Instantaneous power dissipated in the capacitor: $P(t) = i(t)V_c$
  - Energy is defined as power used over a time period:

$$E_c = \int_0^\infty P(t) = \int_0^\infty i(t)V_c\mathrm{d}t = \int_0^\infty C\frac{\mathrm{d}V_c}{\mathrm{d}t}V_c\mathrm{d}t = C\int_0^{V_{DD}} V_c\mathrm{d}V_c$$
$$= \frac{1}{2}CV_{DD}^2$$

Power Dissipation in Logic Gates

- Total energy during one charge/discharge cycle:

$$E = E_{\text{charge}} + E_{\text{discharge}} = 2 \times \frac{1}{2} C V_{DD}^2 = C V_{DD}^2$$

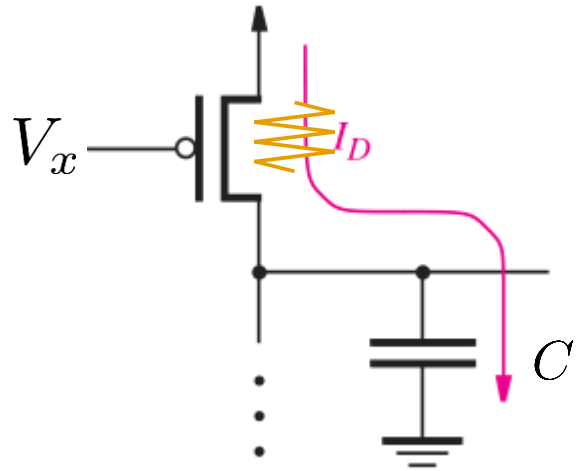


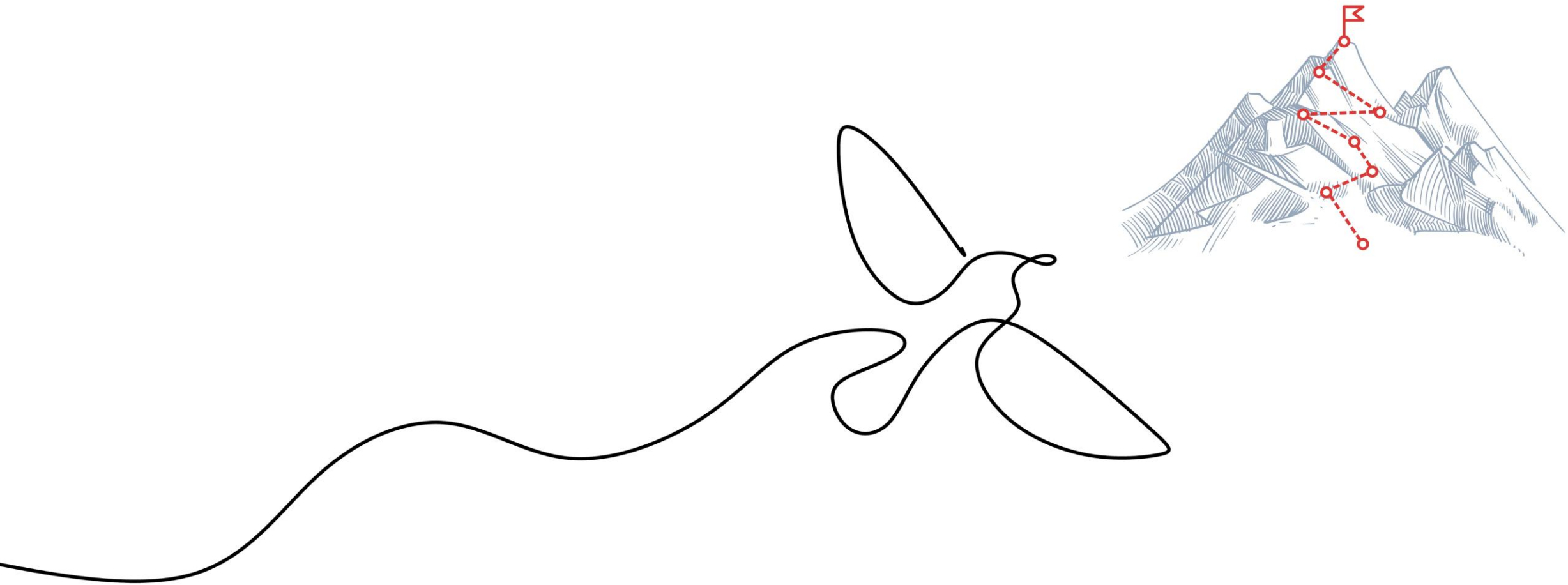
- Power is energy over time:

$$P_D = f C V_{DD}^2$$

Dynamic power

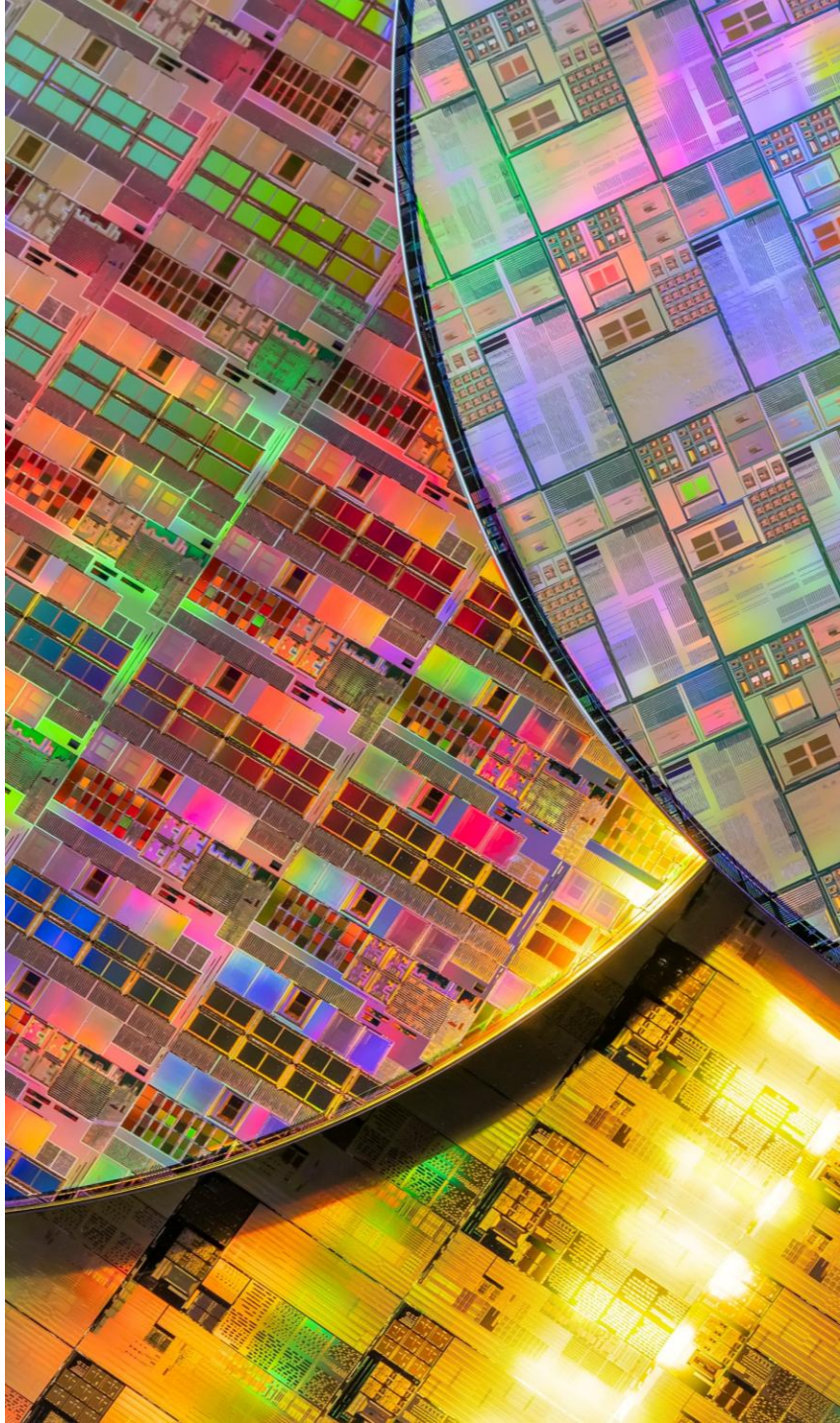
Switching frequency: how frequently C charges and discharges





Hazards

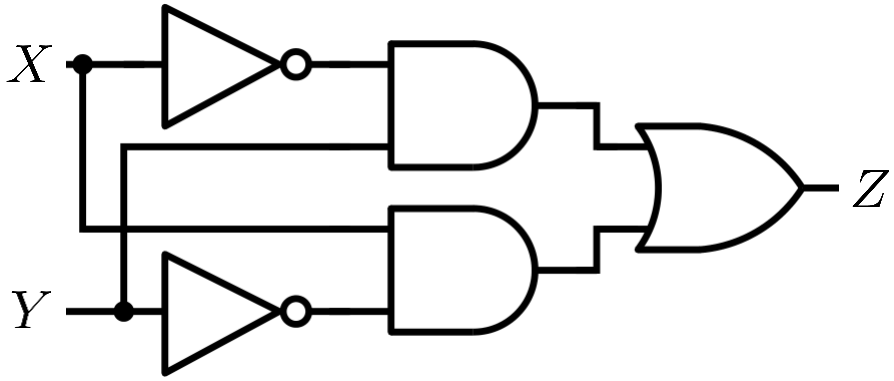
…also known as glitches



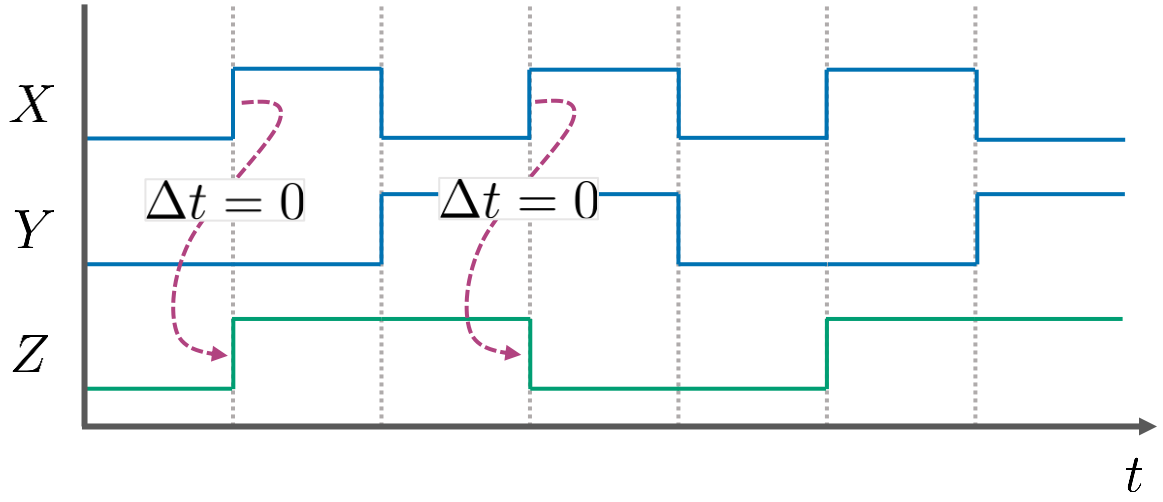
Ideal Timing Waveforms

Zero-Delay Model

- Given the logic circuit and the sequence of inputs shown in the timing diagram, draw the corresponding output waveform
  - Assume **zero delays** (i.e., logic level changes propagate instantaneously)



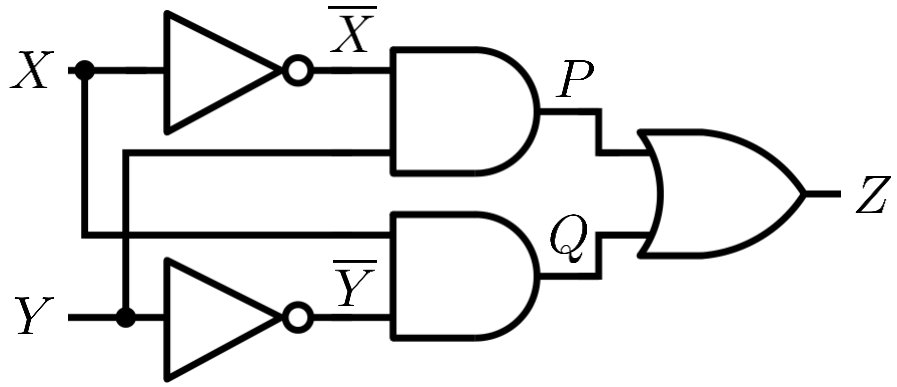
$$Z = \overline{X}\,Y + X\,\overline{Y} = X \oplus Y$$

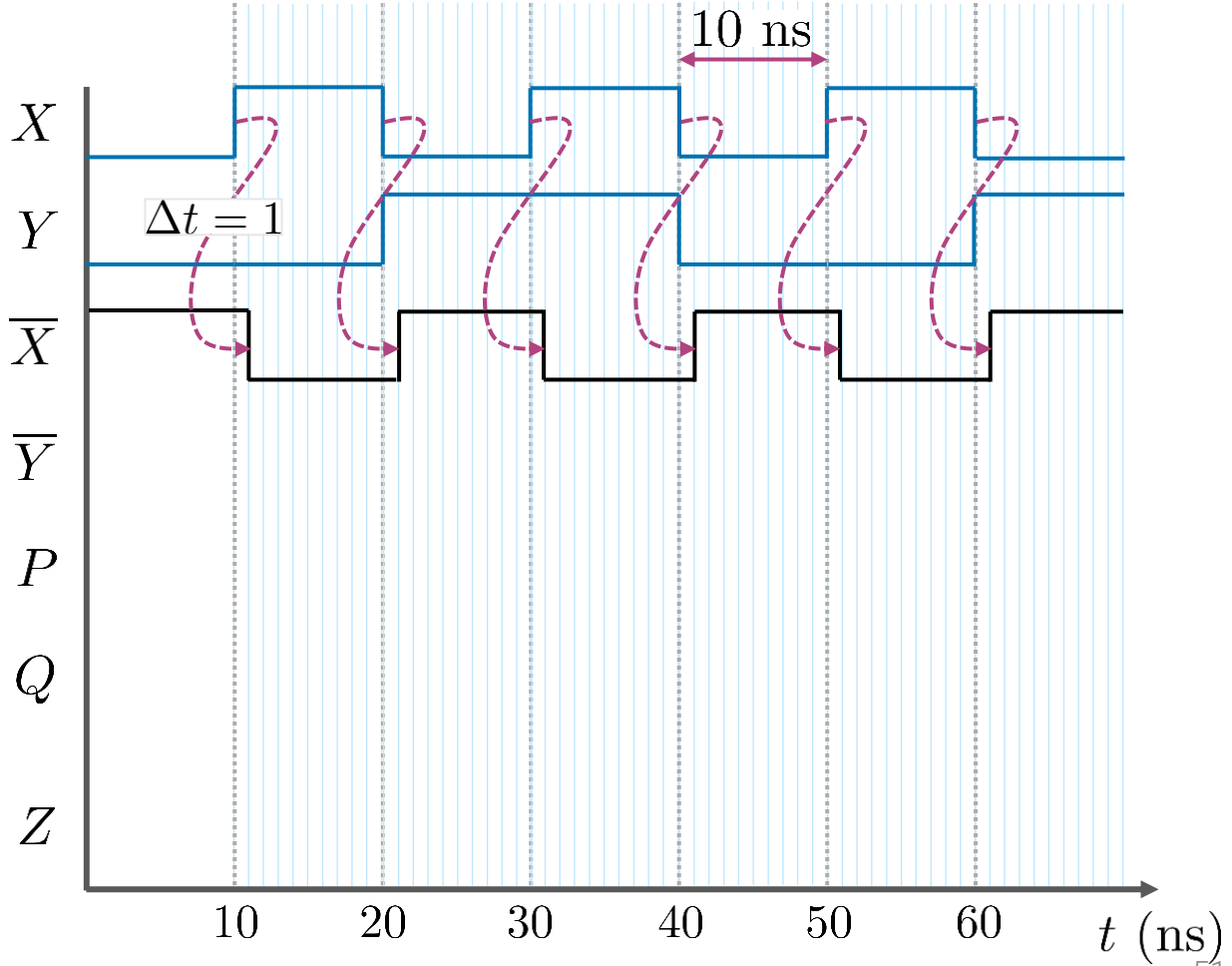


- Such behavior is unrealistic because real circuits have delays

Real Timing Waveforms

- Once again, now assuming wires with zero delays and
  - $d(\text{NOT}) = 1$ ns
  - $d(\text{AND}) = 2$ ns
  - $d(\text{OR}) = 3$ ns





Real Timing Waveforms

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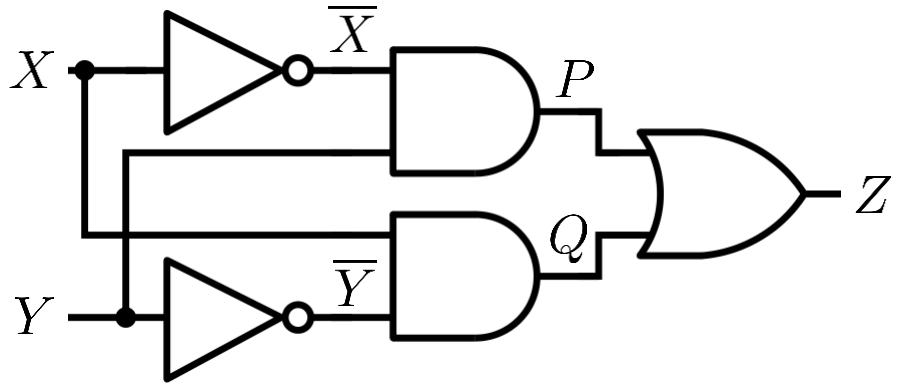

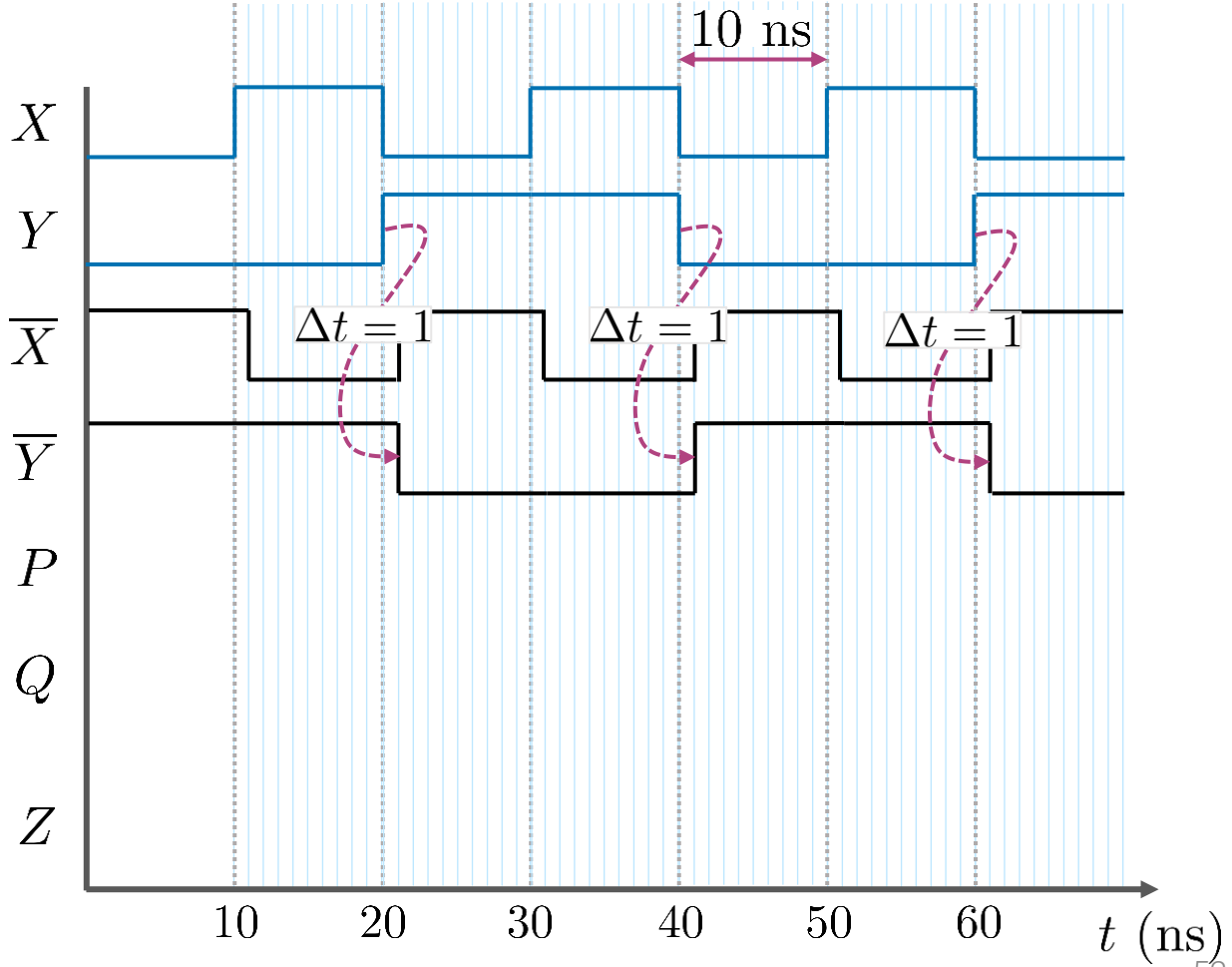

Real Timing Waveforms

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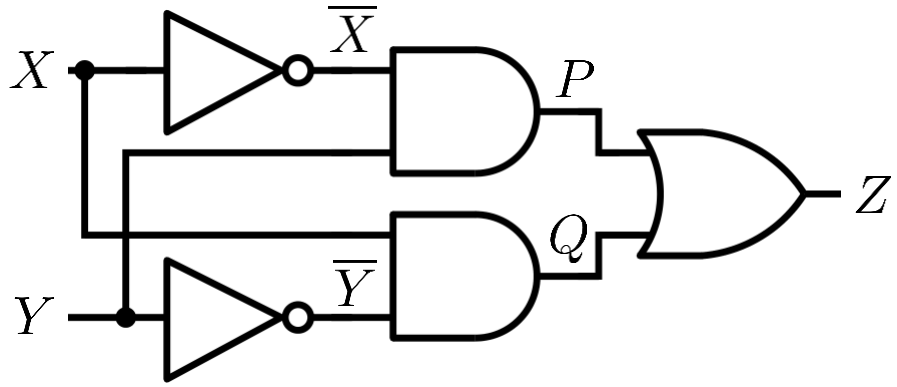

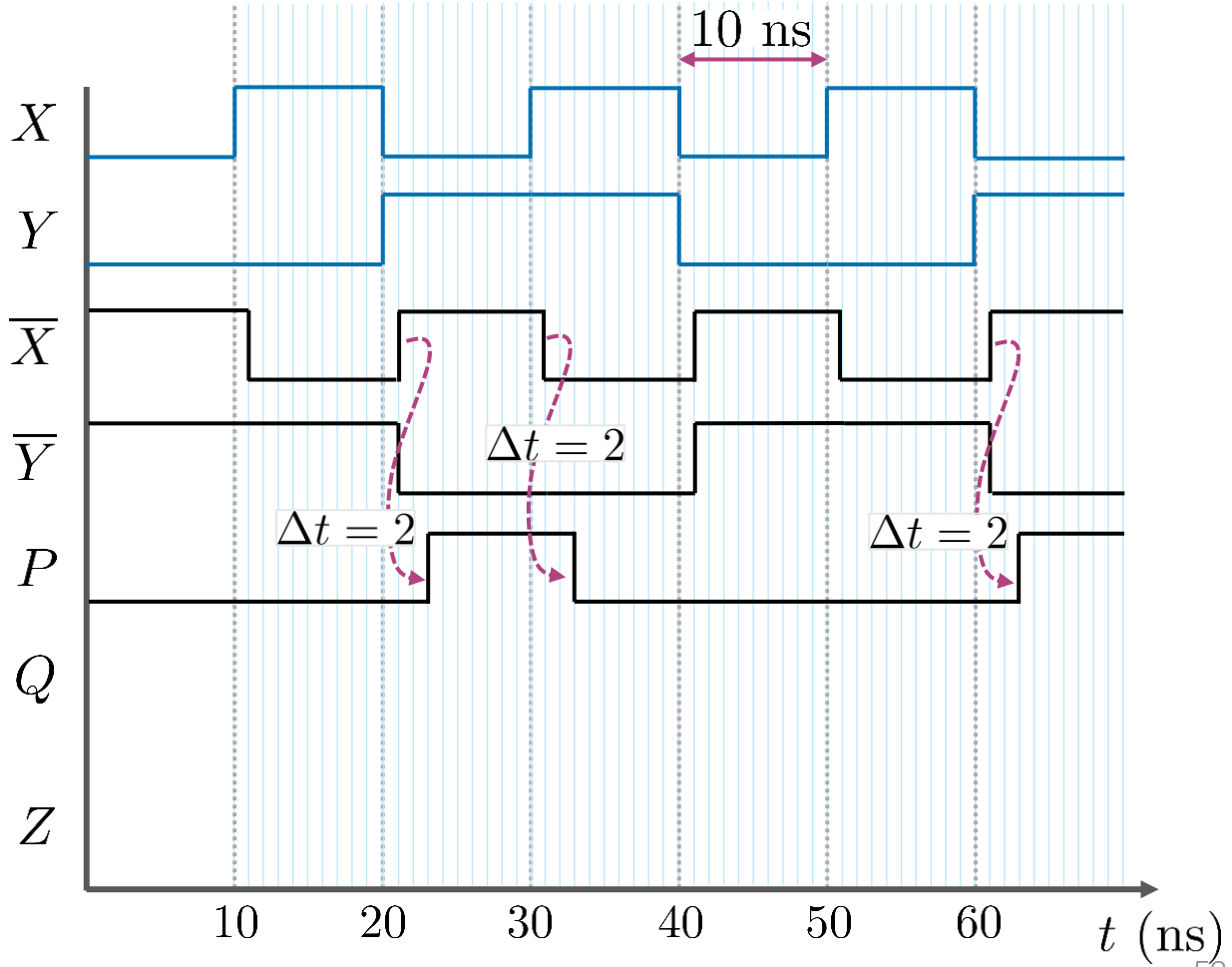

Real Timing Waveforms

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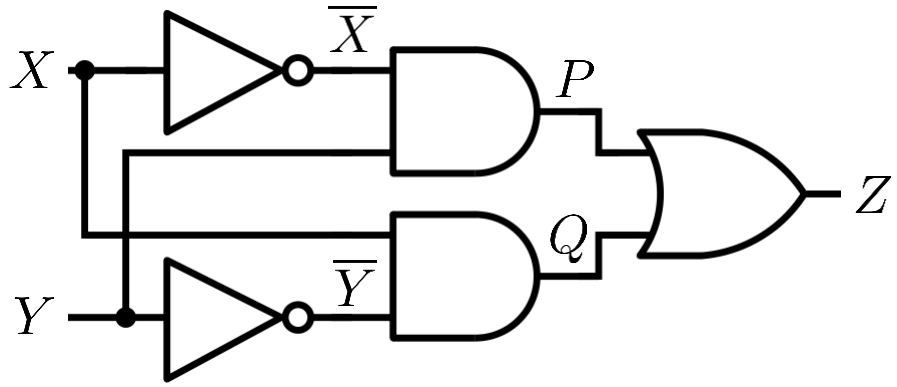

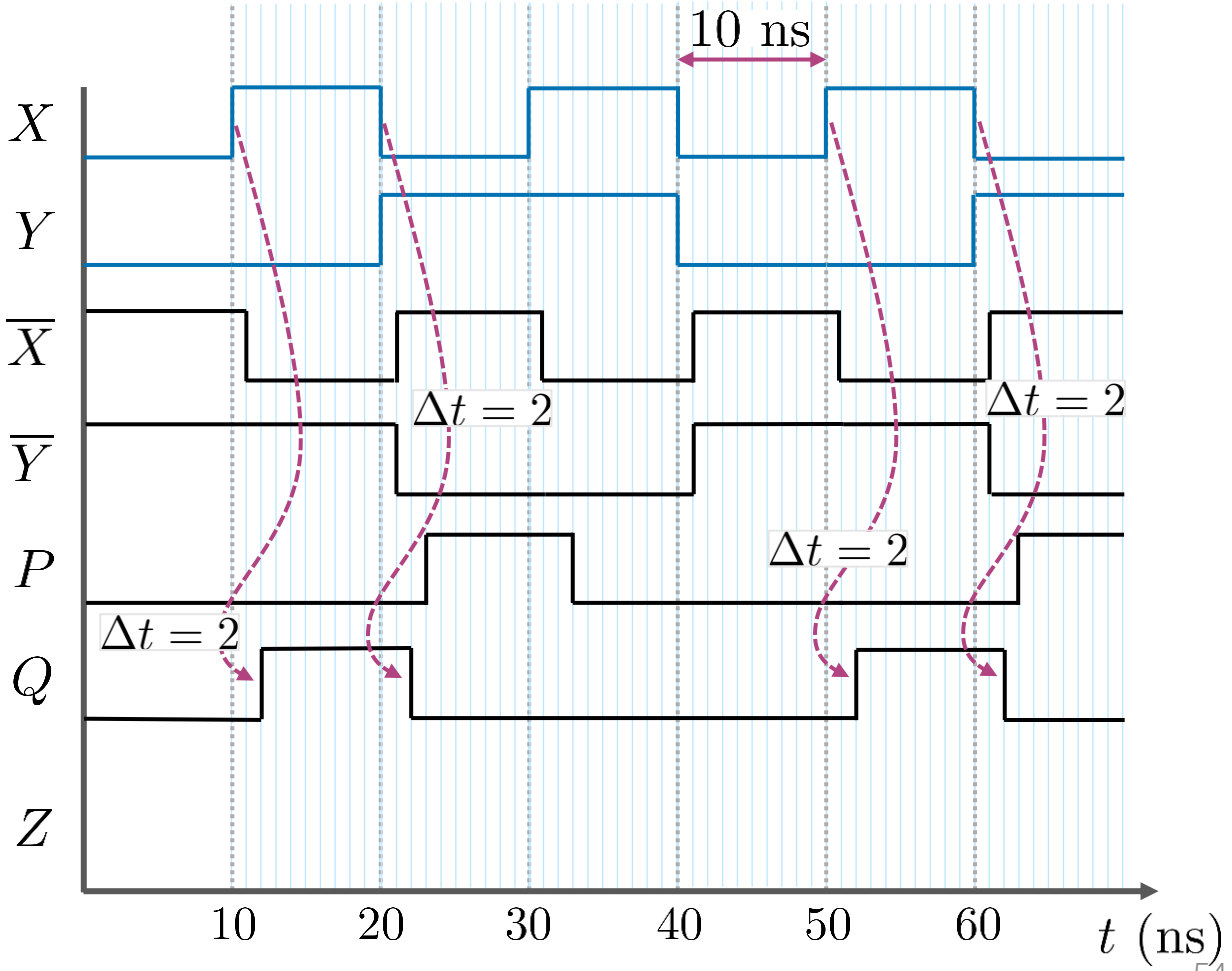

Real Timing Waveforms

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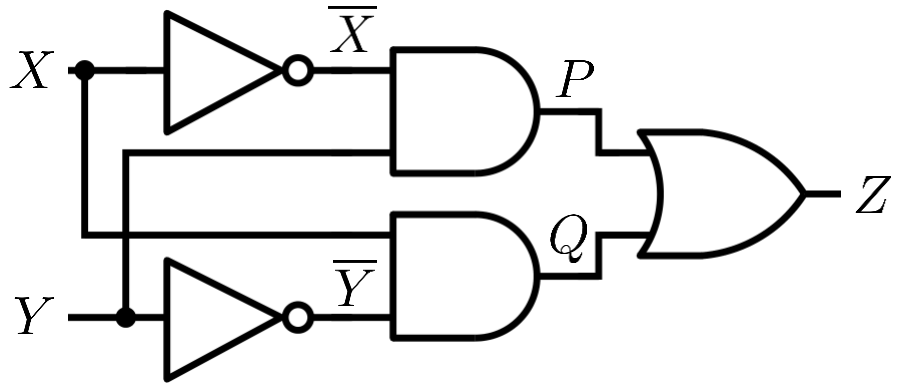
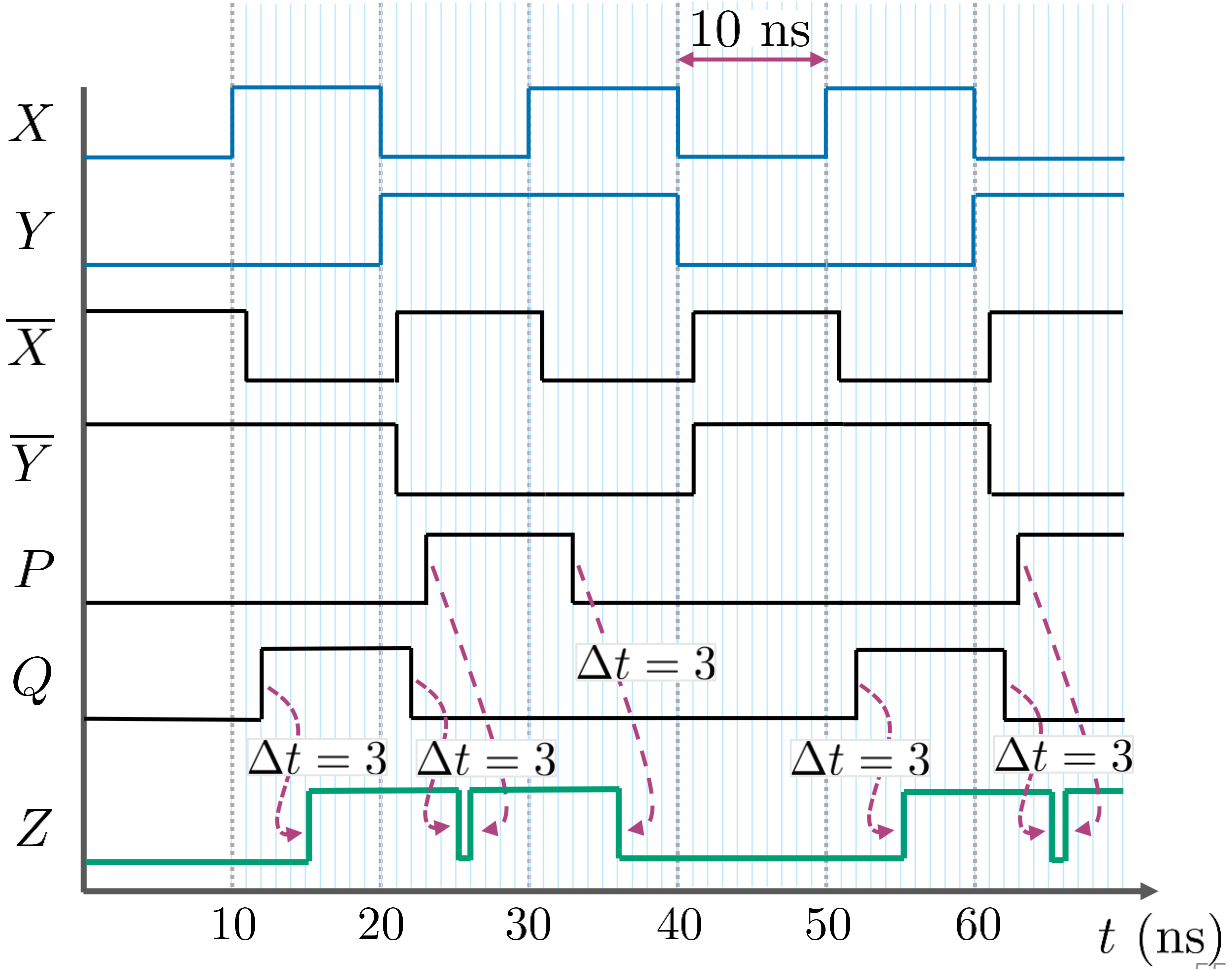
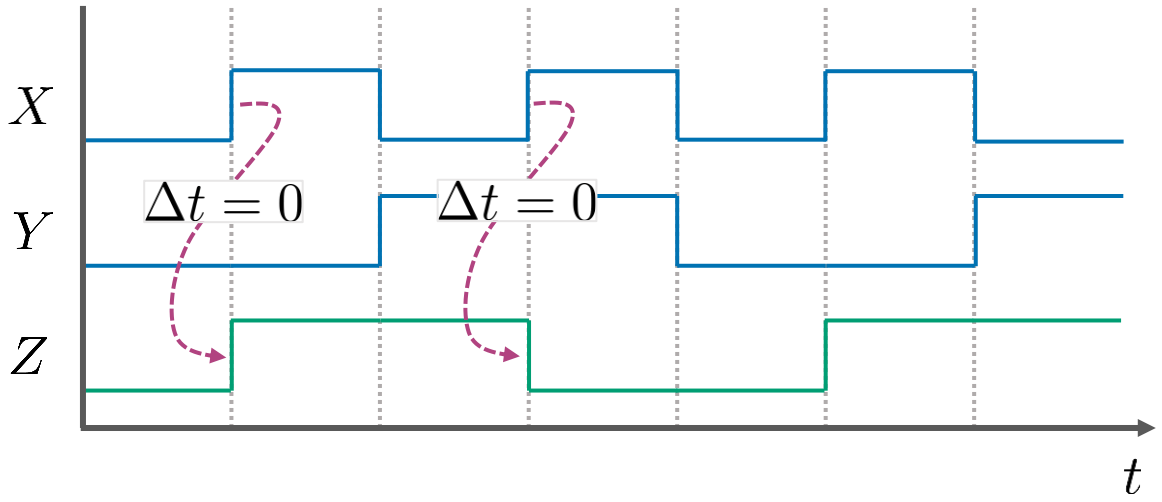




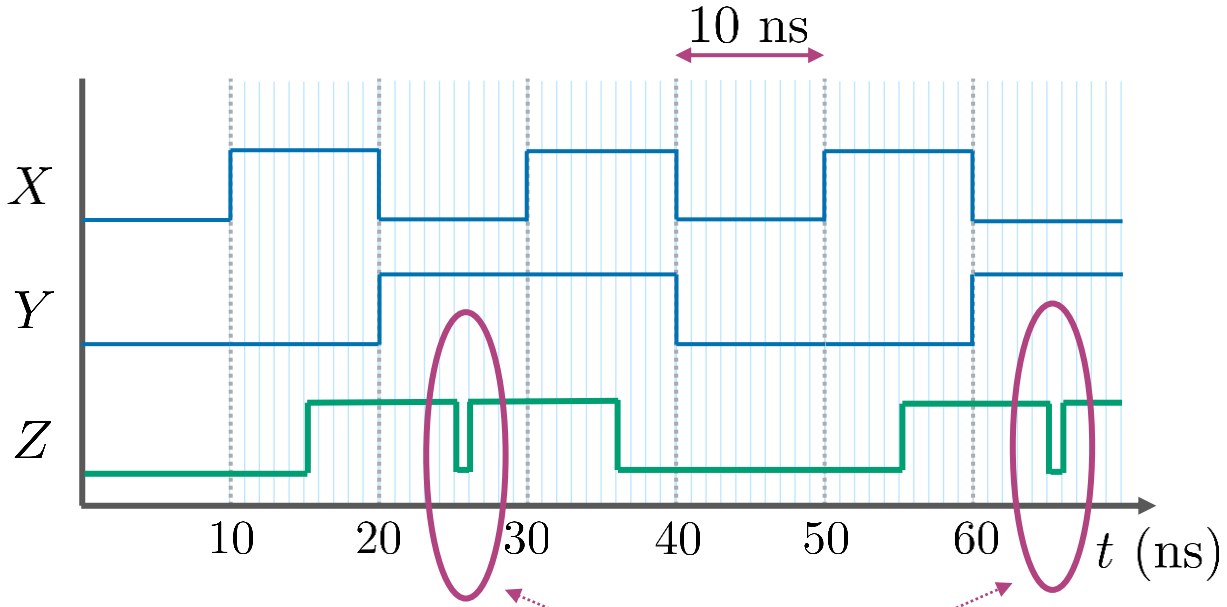
Timing Hazards

Glitches

- Recall: Zero-delay gates



- Real gates



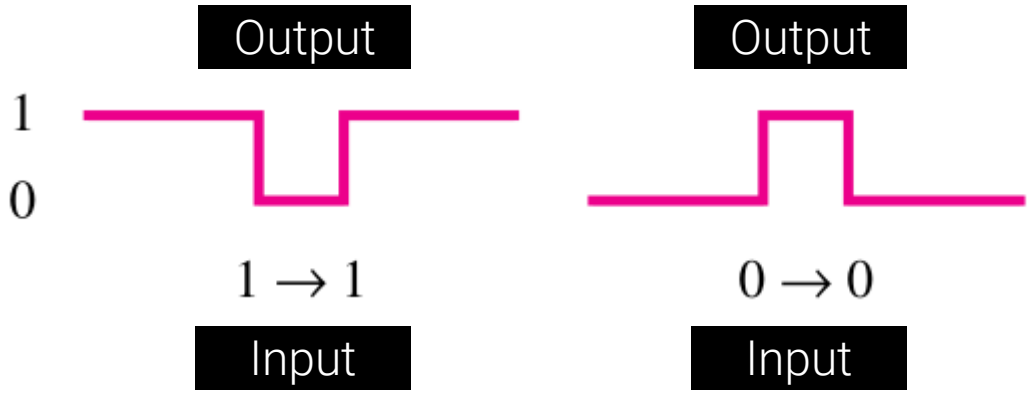
- Delay-caused unwanted level changes are called hazards or glitches; they often cannot be avoided

Unwanted impulses, called hazards or, often, GLITCHES

Static Hazard

Types of Hazards

- A **static hazard** exists if a signal is supposed to **remain** at a particular logic value when an input variable changes its value, but instead, the signal undergoes a **momentary change** in its required value

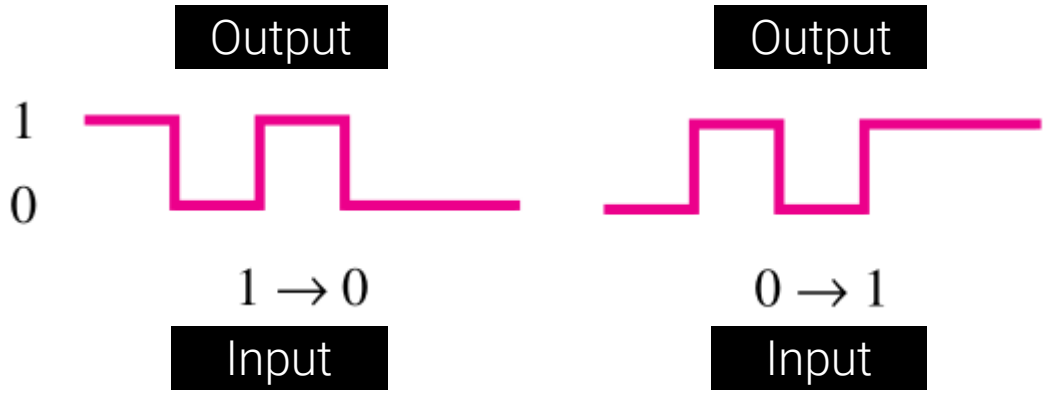


One must be aware of the possibility of hazards happening in real circuits

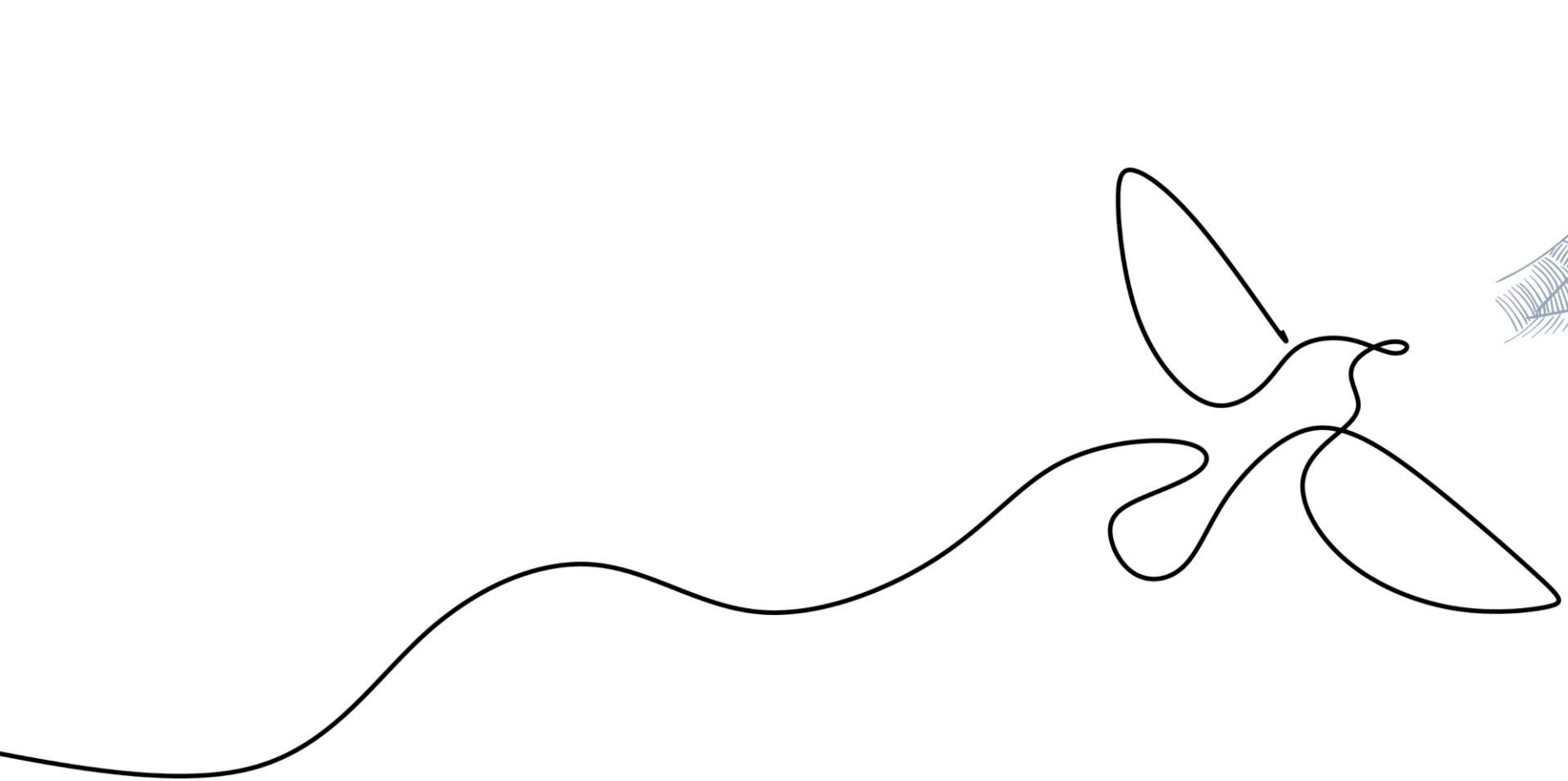
Dynamic Hazard

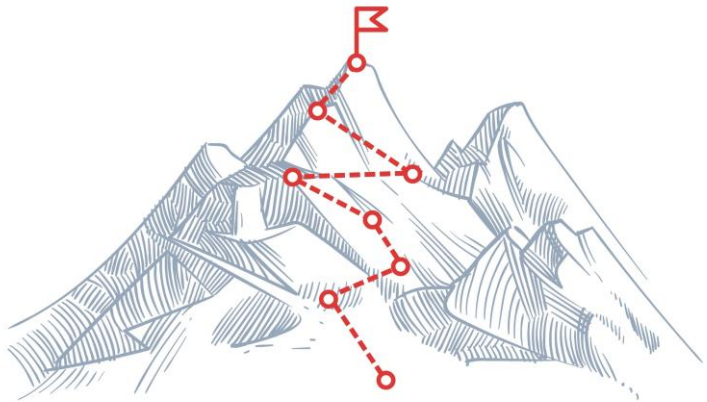
Types of Hazards

- Another type of hazard may occur when a signal is supposed to change: 1→0 or 0→1. A **dynamic hazard** occurs if such a change involves a short oscillation before the signal settles into its new level.



One must be aware of the possibility of hazards happening in real circuits



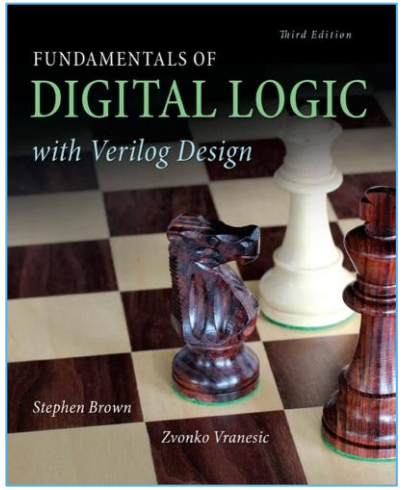


Executive Summary

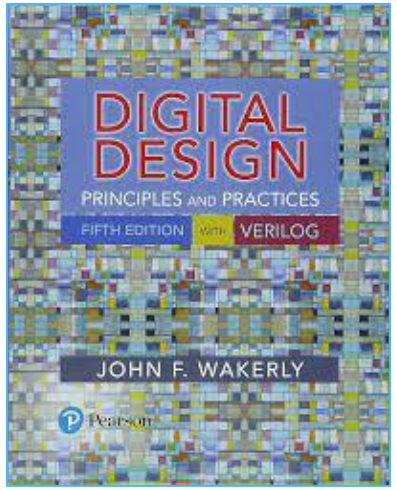
- **Gate delay:** Real gates take time to produce the output logic value
- **Rise and fall time:** Transitions 0⟶1 and 1⟶0 are never instantaneous
- **Glitches:** Real circuits may exhibit hazards (i.e., undesired glitches)
- **Parasitic capacitance:** Gate inputs act as capacitance, loading the outputs of the gates that are driving them and slowing those gates
- **High fan-out is no good:** Load capacitance grows with the fan-out
  - The higher the fan-out, the slower the gate
- **Power consumption matters:** Dynamic power consumption grows
  - linearly with the load capacitance and switching frequency
  - quadratically with the supply voltage

To save power, we lower the operating frequency or voltage or both

Literature



- Appendix B: Implementation Technology
  - B.1-B.4
  - B.8



- Chapter 1: Introduction
  - 1.9